San José State University

Computer Science Department

CS 147, Section 01

Computer Architecture

Spring, 2019

Course and Contact Information

Instructor:	Kaushik Patra
Office Location:	DH 282
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Email:	kaushik.patra@sjsu.edu
Office Hours:	Th 4:30 pm – 5:45 pm
Class Days/Time:	TTh 6:00 pm – 7:15 pm (Sec01)
Classroom:	DH 135
Prerequisites:	CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better)

Course Format

This course uses hybrid style. In general students are expected to have computer systems with internet connection. A tool 'ModelSim' will be used to study hardware operation concepts. The materials are uploaded in Canvas prior to class. Students are encouraged to review the lecture note before coming to class. During class hour it is expected that students bring their laptop with internet connection to download some simulation material to work on during class hour if needed. All the homework and assignments are to be uploaded in Canvas.

Course Description

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Topics:

Hardware Description Languages, Data Representation in Computer Hardware, Computer Arithmetic, Memory Organization, Control Unit Operation and Implementation, Instruction Formats, Pipelining and Vector Processing, Multiprocessing, and RISC Architecture and Principles.

Course Objectives:

- Review the basic Boolean number representation schemes, digital logic gates, and basic combinatorial and sequential circuit structures.
- Introduction to the basic roles and responsibilities for each of the major hardware components of a computer.
- Review the need to use a memory hierarchy, perform memory management, and to explain to them the various memory management techniques and their tradeoffs.
- Review implementation of the fundamental mathematical operations such as addition, subtraction, multiplication, and division and optimization with Boolean operands.
- Review tradeoffs between complex instruction set computers (CISC) and reduced instruction set computers (RISC).
- Review non-classical architectures such as parallel processors and pipelined machines which are used to accelerate hardware performance without impacting legacy sequential software programming languages or techniques.
- Introduction to computer-aided design tools and hardware description languages useful to computer architects in performing functional verification and performance measurements of digital systems.
- Review operation of hardware and software working synergistically together.

Learning Outcomes and Course Goals

Course Goal:

To examine alternative organizations and architectures associated with the implementation of basic computer hardware functions such as the memory hierarchy and its management, central processing unit (CPU) and arithmetic logic unit (ALU), instruction sets, and RISC.

Course Learning Outcomes (CLO):

Upon successful completion of this course, students should be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.

- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.
- Appreciate how computer-aided design tools and hardware description languages can be used to verify and measure the performance of hardware designs

BS in Computer Science Program Outcomes Supported:

These are the BSCS Program Outcomes supported by this course:

a) An ability to apply knowledge of computing and mathematics to solve problems.

b) An ability to analyze a problem, to identify and define the computing requirements appropriate to its solution

c) An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs

d) An ability to use current techniques, skills, and tools necessary for computing practice

e) An ability to apply mathematical foundations, algorithmic principles, and computer science theory in the modeling and design of computer-based systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

Required Texts/Readings – can be rented or bought used/new from SJSU bookstore

Textbook

COMPUTER ORGANIZATION and DESIGN | Edition: 5
Author: DAVID A. PATTERSON
ISBN:9780124077263
Publication Date:10/10/2013
Publisher:ELSEVIER

Other Readings

COMPUTER ARCHITECTURE | Edition: 5TH 12
Author: HENNESSY
ISBN: 9780123838728
Publication Date: 09/29/2011
Publisher: ELSEVIER

LOGIC & COMPUTER DESIGN FUNDAMENTALS
Author: MANO & KIME
ISBN: 9780131989269
Publication Date: 06/15/2007
Publisher: PEARSON

COMPUTER ORGANIZATION and ARCHITECTURE | Edition: 9TH 13
Author: STALLINGS
ISBN: 9780132936330
Publication Date: 03/15/2012
Publisher: PEARSON

VERILOG HDL-W/CD | Edition: 2ND 03
Author: PALNITKAR
ISBN: 9780130449115
Publication Date: 03/10/2003
Publisher: PEARSON

Other technology requirements / equipment / material

You will be **required** to bring a wireless laptop to all classes.

Course Requirements and Assignments

- Each student is expected to be present, punctual, and prepared at every scheduled class and lab session. It is assumed that the students already have basic knowledge of digital Boolean logic and fundamentals of assembly language machine programming.
- Attendance is **NOT** optional. Individual participation is also required. There will be no make-ups for missed midterm or assignments, unless any special arrangements is made with the instructor beforehand.
- All student **must complete** the ***Syllabus agreement*** through by ***Jan 26, 2019 11:59 pm***. Any one **failed** to do so will be **dropped** from the class. The link to this agreement will be sent to individual email as '***[CS147,01] PreReq-Survey***' from https://sjsu.qualtrics.com.
- There will be **3 individual projects, 4 quizzes**, one **midterm** and **final exam**. All quizzes and projects should be submitted through Canvas. **No scanned copy** of handwritten solution is allowed. Allowed document type is **PDF** only.

Project report should contain the following.

- Introduction containing objective.
- Requirement.

- Design and Implementation.
- Testing
- Conclusion
- Make sure to
    1. Include clear diagrams for requirement and design.
    2. Include code snippet to explain implementation.
    3. Include screen shots of testing results.
    4. Upload source code and test program as zip archive.

Project reports are encouraged to be submitted in IEEE format.
[http://www.ieee.org/conferences_events/conferences/publishing/templates.html]

10% of the obtained marks in project will be awarded as extra points in project evaluation if report submitted in proper IEEE format.

Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/studying, or course related activities, including but not limited to internships, labs, and clinical practica. Other course structures will have equivalent workload expectations as described in the syllabus.

LockDown Browser + Webcam Requirement

This course requires the use of LockDown Browser and a webcam for online quizzes. The webcam can be the type that's built into your computer or one that plugs in with a USB cable.

Watch this brief video to get a basic understanding of LockDown Browser and the webcam feature.

https://www.respondus.com/products/lockdown-browser/student-movie.shtml

Download Instructions
Download and install LockDown Browser from this link:

https://download.respondus.com/lockdown/download.php?id=967937270

Once Installed

- Start LockDown Browser
- Log into to Canvas
- Navigate to the quiz

Note: You won't be able to access a quiz that requires LockDown Browser with a standard web browser. If this is tried, an error message will indicate that the test requires the use of LockDown Browser. Simply start LockDown Browser and navigate back to the exam to continue.

Guidelines
When taking an online quiz, follow these guidelines:

- Ensure you're in a location where you won't be interrupted
- Turn off all other devices (e.g. tablets, phones, second computers) and place them outside of your reach
- Before starting the test, know how much time is available for it, and also that you've allotted sufficient time to complete it
- Clear your desk or workspace of all external materials not permitted - books, papers, other devices

- Remain at your computer for the duration of the test
- If the computer, Wi-Fi, or location is different than what was used previously with the "Webcam Check" and "System & Network Check" in LockDown Browser, run the checks again prior to the exam
- To produce a good webcam video, do the following:
    - Avoid wearing baseball caps or hats with brims
    - Ensure your computer or device is on a firm surface (a desk or table). Do NOT have the computer on your lap, a bed, or other surface where the device (or you) are likely to move
    - If using a built-in webcam, avoid readjusting the tilt of the screen after the webcam setup is complete
    - Take the exam in a well-lit room, but avoid backlighting (such as sitting with your back to a window)
- Remember that LockDown Browser will prevent you from accessing other websites or applications; you will be unable to exit the test until all questions are completed and submitted

Getting Help
Several resources are available if you encounter problems with LockDown Browser:

- The Windows and Mac versions of LockDown Browser have a "Help Center" button located on the toolbar. Use the "System & Network Check" to troubleshoot issues. If an exam requires you to use a webcam, also run the "Webcam Check" from this area
- Respondus has a Knowledge Base available from support.respondus.com. Select the "Knowledge Base" link and then select "Respondus LockDown Browser" as the product. If your problem is with a webcam, select "Respondus Monitor" as your product
- If you're still unable to resolve a technical issue with LockDown Browser, go to support.respondus.com and select "Submit a Ticket". Provide detailed information about your problem and what steps you took to resolve it

Final Examination or Evaluation

There shall be an appropriate final examination and evaluation at the scheduled time as indicated in University calendar, unless specifically exempted by the college dean who has curricular responsibility of the course. The examination is expected to have descriptive, problem analysis and problem solving style questions to answer.

Grading Information

1. Project carries **50%** towards final score. Average of 3 score from projects will be contributed.
2. Quiz carries **20%** towards final score. Average of 4 score from quiz will be contributed.
3. Midterm carries **10%** towards final score.
4. Final carries **20%** towards final score.

Submission is allowed till **11:59 pm on due date**. Zero delay tolerance for the submission, i.e. NO late submission is permitted, unless you make special arrangements with your instructor beforehand.

You will receive a numeric score for the midterm, the final, each of the total homework, and each project submission. Letter grade, which is your class grade, will be obtained by adding the numeric scores and weighing with the percentages given below. Fraction in percentage will be converted into nearest integer value ('>= 0.5' will be moved to next integer number, '< 0.5' will be moved to previous integer number).

A+ = 100-97%	A = 96-93%	A- = 92-90%
B+ = 89-87%	B = 86-83%	B- = 82-80%

C+ = 79-77%	C = 76-73%	C- = 72-70%
D+ = 69-67%	D = 66-63%	D- = 62-60%
F = 59-0% Failure		

Classroom Protocol

1. **You must come to class on time!** Students entering the classroom late disrupt the lecture and / or the students already in class who may be engaged in lab or discussion. Late students will not be accepted in class.

2. If you miss a lecture you are still responsible for any material discussed or assignments given. A large portion of each class will be used for hands-on lab / discussion. All students are expected to participate in class activities. Students who are often absent will find themselves at a disadvantage during the tests.

3. No audio / video recording or photography in the classroom without prior permission of instructor.

4. It is individual **student responsibility** to **check validity** of their homework, assignment, project, submission (format error, blank files, corrupted files, and many more such) and re-submit within deadline if needed. Once the grading is started there will be no consideration for resubmit. ***If the submission found to have any logistics issue at grading time (format error, blank files, corrupted files, and many more such) it will be evaluated as 0***.

5. No personal discussion or cell phone activity during class time. Please set the cell phone on **silent/vibrate** mode.

6. All e-mail communication to the instructor must have the subject line start with **[CS147,01]**

7. Email to be sent to the instructor's SJSU email ID (kaushik.patra@sjsu.edu) only.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

Course Schedule – *subject to change by instructor with due notice.*

Date	Lecture	Lab	Notes
01/24/19	Intro CS147		
01/29/19	Introduction to Computer, Basic Instruction Set, ALU	Tool setup	**Project I Posted** **Submit Prerequisite Survey & Syllabus Agreement**
01/31/19	Clock, Memory, Controller, Von-Neumann Architecture, System Software	Hierarchical Models	
02/05/19	Digital Synthesis, Number Representation	Simulation Project	Last date to drop (Feb 5)
02/07/19	Boolean Algebra I	Data Flow Modeling I	Add code will be supplied/Last date to add course (Feb12)
02/12/19	Boolean Algebra II	Data Flow Modeling II	Project II Posted.
02/14/19	Comb/Seq Logic I	Memory Modeling	**Quiz-01 (Feb 15-16)**
02/19/19	Comb/Seq Logic II	Project 02 Discussion	**Project I Submission**
02/21/19	Seq Logic Design, Common Digital Components I	Behavioral Modeling I	
02/26/19	Common Digital Components II	Behavioral Modeling II	**Project 02 Milestone 1 Submission**
02/28/19	Addition / Subtraction Logic Circuit	Behavioral Modeling III	
03/05/19	Multiplication / Division Logic Circuit	Behavioral Modeling IV	**Project 02 Milestone 2 Submission**
03/07/19	Putting Together a Microprocessor – I	Project 02	
03/12/19	Putting Together a Microprocessor – II	Project 02	**Project 02 Milestone 3 Submission**
03/14/19	Midterm Review	Project 02	**Quiz-02 (Mar 15-16)**
03/19/19	**Midterm Exam**		
03/21/19	Instruction Set Architecture, RISC/CISC	Project 02	**Project 02 Milestone 4 Submission**
03/26/19	Processor Performance Measurement	Gate Level Modeling I	Project III Posted
03/28/19	Pipeline Architecture I	Gate Level Modeling II	**Project II Submission**
04/02/19	**Spring Break (April 01-05)**		
04/04/19			
04/09/19	Pipeline Architecture II	Gate Level Modeling III	
04/11/19	ILP, Hardware Threading	Project 03 Part I	**HW02 Submission / HW03 Posted**
04/16/19	Parallel Processing I	Project 03 Part II	
04/18/19	Parallel Processing II	Project 03 Part III	**Quiz-03 (Apr 19-20)**
04/23/19	Memory Hierarchy, Cache Memory I	Project 03 Part IV	
04/25/19	Cache Memory II	Project 03	
04/30/19	Cache Memory III	Project 03	**Project III Submission**
05/02/19	Cache Memory IV	Project 03	
05/07/19	Virtual Memory Concept		
05/09/19	Review-01		**Quiz-04 (May 10-11)**
05/14/19	Review-02		
05/16/19	**Final Exam @ 5:15pm – 7:30pm**		