Binh Q. Le

Phone: (408)-924-3915

Email(s): binh.q.le@sjsu.edu

EDUCATION

- **Ph. D.** in Electrical Engineering, Stanford University, 1/2004
- **M.S.** in Electrical Engineering, Stanford University, 6/1999
- **B.S.** in Electrical Engineering and Computer Science, U.C. Berkeley, 5/1994

PROFESSIONAL EXPERIENCE

- **San Jose State University, Electrical Engineering Department** **8/2019 to present**
  - Assistant Professor 8/2019 to present

- **Stanford University, Electrical Engineering Department** **1/2016 to 9/2019**
  - Senior Research Engineer 9/2016 to 9/2019
  - Lecturer for EE 271 (Introduction to VLSI systems) 1/2016 - 3/2016

  Responsibilities: Work directly with Ph.D. students (and/or supervise for the tapeout) on the following projects: Embedded/Nano Systems with RRAM non-volatile memory targeting machine learning applications, Cross-Layer Resilience in Low-Voltage Digital Systems, Sensory Particles for Optical Telemetry, Carbon Nanotube Ring Oscillator. Contribute ideas/Attend meetings for Retina Electro-Neural Interface project.

- **SanDisk Corporation, Milpitas, CA** **9/2004 to 9/2016**
  - Director, Design Engineering 2013 - 2016
  - Senior Design Manager 2009 - 2013
  - Design Manager II 2004 - 2009

  Responsibilities: Lead large design teams at different geography locations (US, Japan and India) to develop Flash memory products, from design concept to mass production. Interface closely with system, test, device, product, characterization, and applications teams.

- **Advanced Micro Devices, Inc., Sunnyvale, CA** **6/1994 to 9/2004**
  - Section Design Manager 2003 - 2004
  - Member of Technical Staff 2002 - 2003
  - Senior Design Engineer 1998 - 2002
  - Design Engineer II 1996 - 1998
  - Design Engineer I 1994 - 1996

  Responsibilities: Lead design teams to work on different projects using various technologies, and directly work on many design blocks (sensing, row/column decoding, charge pumps and regulators, high-speed datapath, program/erase algorithms and state machines, etc.)

SKILLS

- Computer Languages: C, C++, Java, Python, Mathlab, Assembly, Perl.
- Applications: Verilog, Design Compiler RTL Synthesis, PrimeTime, SystemVerilog Assertions, SystemVerilog Testbench, SystemVerilog Verification using UVM, IC Compiler Block-level Implementation, IC Compiler SoC Design Planning, PrimeRail, Cadence Opus, Design Architect, HSPICE, Finesim.
- Familiar with ARM, MIPS, RISC processors.

HONORS AND AWARDS

- IEEE Senior Member 2019
- Holding 59 U.S. Patents (leading inventor of 34)
- Inventor Award, SanDisk Corporation 2012
- Prolific Inventor Award, Advanced Micro Devices, Inc. 2002
- Graduated with high honors from University of California, Berkeley 1994
- Berkeley Regents' Scholarship 1992-1994

PUBLICATIONS AND PAPERS

10. E.R. Hsieh, ..., **B.Q. Le**, et al., "High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning", 2019 International Electron Devices Meeting (IEDM 2019).
9. **B. Le** *et al*., "Resistive RAM with Multiple Bits per Cell: Array-Level Demonstration of 3 Bits per Cell," IEEE Transactions on Electron Devices Journal, vol. 66 Issue 1, Jan. 2019 (Digital Object Identifier: 10.1109/TED.2018.2879788). Also in the Research highlight part, Nature Electronics Journal, vol. 2, Feb. 2019.
8. Tony F. Wu, **B. Le** *et al*., "A 43pJ/cycle Non-volatile Microcontroller with 4.7us Shutdown/Wake-up integrating 2.3 bits-per-cell Resistive RAM and Resilience Techniques." 2019 International Solid-State Circuits Conference (ISSCC 2019).
7. E. Cheng, …, **Binh Le**, *et al*., "Cross-Layer Resilience in Low-Voltage Digital Systems: Key Insights," *2017 IEEE International Conference on Computer Design (ICCD)*, Boston, MA, 2017, pp. 593-596.
6. Alessandro Grossi, …, **Binh Le**, *et al*., "Resistive RRAM Endurance: Array-level Characterization and Correction Techniques Targeting Deep Learning Application," IEEE Transactions on Electron Devices Journal, vol. 66, Mar. 2019 (Digital Object Identifier: 10.1109/TED.2019.2894387).
5. Y. Li, …, **Binh Le**, *et al*., "128Gb 3b/cell NAND flash memory in 19nm technology with 18MB/s write rate and 400Mb/s toggle mode," *2012 IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2012, pp. 436-437.
4. C. Trinh, …, **B. Le**, *et al*., "A 5.6MB/s 64Gb 4b/Cell NAND Flash memory in 43nm CMOS," *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, San Francisco, CA, 2009, pp. 246-247,247a.

3. R. Cernea, …, **Binh Le**, *et al*., "A 34MB/s-Program-Throughput 16Gb MLC NAND with All-Bitline Architecture in 56nm," *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, San Francisco, CA, 2008, pp. 420-624.

2. K. Kanda, …, **Binh Le**, *et al*., "A 120mm^2 16Gb 4-MLC NAND Flash Memory with 43nm CMOS Technology," *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, San Francisco, CA, 2008, pp. 430-625.

1. **B. Q. Le**, *et al*., "Virtual-ground sensing techniques for a 49-ns/200-MHz access time 1.8-V 256-Mb 2-bit-per-cell flash memory," in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 2014-2023, Nov. 2004.

PATENTS

60. **B. Le**, A. Grossi, E. Vianello, T. Wu, G. Lama, E. Beigné, H.-S. Philip Wong, S. Mitra, "Multi-bit per cell Resistance Distribution Control for Fast, Efficient Read and Program for Resistive RAM," Provisional Patent Application (S18-116-PROV), 4/2018.
59. M. Mui, Y. Dong, **B. Le**, D. Dutta, "Partial speed and full speed programming for non-volatile memory using floating bit lines", US patent 8,081,514 (Issued on December 20, 2011).
58. T.-H. Kuo, N. Leong, N. Yang, G. Wang, A. Lee, S. Chandra, M. Van Buskirk, J. Chen, D. Hamilton, and **B. Q. Le**, "High performance flash memory device capable of high density data storage", US Patent 7,443,732 (Issued on October 28, 2008).
57. **B. Q. Le**, and P.-L. Chen, "Method and system for defining a redundancy window around a particular column in a memory array", US Patent 7,076,703 (Issued on July 11, 2006).
56. E. Runnion, T.-C. Yang, **B. Q. Le**, S. Yamada, D. Hamilton, M.-H. Shieh, P.-L. Chen, and K. Kurihara, "Method to obtain temperature independent program threshold voltage distribution using temperature dependent voltage reference", US Patent 6,944,057 (Issued on September 13, 2005).
55. D. Hamilton, E. Ajimine, **B. Q. Le**, E. Hsia, and K. Tanpaijo, "Erase method for a dual bit memory cell", US Patent 6,901,010 (Issued on May 31, 2005).
54. **B. Q. Le**, C.T. Ly, L. Cleveland, and P.-L. Chen, "Fast bandgap reference circuit for use in a low power supply A/D booster", US Patent 6,894,473 (Issued on May 17, 2005).
53. **B. Q. Le**, L. Cleveland, and P. Chen, "Cascode amplifier circuit for generating and maintaining a fast, stable and accurate bit line voltage", US Patent 6,885,250 (Issued on April 26, 2005).
52. **B. Q. Le**, C.T. Ly, L. Cleveland, and P.-L. Chen, "Fast, accurate and low power supply voltage booster using A/D converter", US Patent 6,798,275 (Issued on September 28, 2004).
51. K. Kurihara, **B. Q. Le**, P.-L. Chen, D. Hamilton, and E. Hsia, "Non-volatile memory read circuit with end of life simulation" US Patent 6,791,880 (Issued on September 14, 2004).
50. Y. He, E. Runnion, Z. Liu, M. Randolph, D. Hamilton, P. Chen, and **B. Q. Le**, "Pre-charge method for reading a non-volatile memory cell", US Patent 6,788,583 (Issued on September 7, 2004).
49. **B. Q. Le**, L. Cleveland, and P. Chen, "Buffer driver circuit for producing a fast, stable, and accurate reference voltage", US Patent 6,781,417 (Issued on August 24, 2004).
48. **B. Q. Le**, M. Achter, L. Cleveland, and P. Chen, "Selection circuit for accurate memory read operations", US Patent 6,768,679 (Issued on July 27, 2004).
47. **B. Q. Le**, L. Cleveland, and P.-L. Chen, "Cascode amplifier circuit for producing a fast, stable and accurate bit line voltage", US Patent 6,768,677 (Issued on July 27, 2004).

46. **B. Q. Le**, P.-L. Chen, and R. Tsao, "Circuit for fast and accurate memory read operations", US Patent 6,744,674 (Issued on June 1, 2004).
45. M. Randolph, D. Hamilton, **B. Q. Le**, and W. Zheng, "Method for fabricating nitride memory cells using a floating gate fabrication process", US Patent 6,743,677 (Issued on June 1, 2004).
44. **B. Q. Le**, M. Achter, L. Cleveland, and P.-L. Chen, "Circuit for accurate memory read operations", US Patent 6,731,542 (Issued on May 4, 2004).
43. **B. Q. Le**, M. Chung, and P.-L. Chen, "Refresh scheme for dynamic page programming", US Patent 6,700,815 (Issued on March 2, 2004).
42. **B. Q. Le**, and P.-L. Chen, "Algorithm dynamic reference programming", US Patent 6,690,602 (Issued on February 10, 2004).
41. **B. Q. Le**, and P.-L. Chen, "Method for improving read margin in a flash memory device", US Patent 6,643,177 (Issued on November 4, 2003)
40. **B. Q. Le**, M. Yano, and S. Yachareni, "Voltage boost circuit using supply voltage detection to compensate for supply voltage variations in read mode voltage", US Patent 6,535,424 (Issued on March 18, 2003).
39. S. Hollmer, J. Pawletko, and **B.Q. Le**, "Method and apparatus for adjusting on-chip current reference for EEPROM sensing", US Patent 6,525,966 (Issued on February 25, 2003).
38. **B. Q. Le**, and P.-L. Chen, "Negative pump regulator using MOS capacitor", US Patent 6,515,903 (Issued on February 4, 2003).
37. **B. Q. Le**, P.-L. Chen, M. Van Buskirk, S. Yachareni, M. Chung, K. Kurihara, and S. Hollmer, "Drain side sensing scheme for virtual ground flash EPROM array with adjacent bit charge and hold", US Patent 6,510,082 (Issued on January 21, 2003).
36. S. Yachareni, D. Hamilton, **B. Q. Le**, and K. Kurihara, "Soft program and soft program verify of the core cells in flash memory array", US Patent 6,493,266 (Issued on December 10, 2002).
35. **B. Q. Le**, and P.-L. Chen, "Modulated charge pump with uses an analog to digital converter to compensate for supply voltage variations", US Patent 6,424,570 (Issued on July 23, 2002).
34. S. Yachareni, K. Kurihara, **B. Q. Le**, and M. Chung, "Ceiling test mode to characterize the threshold voltage distribution of over programmed memory cells", US Patent 6,370,061 (Issued on April 9, 2002).
33. J. Pawletko, **B. Q. Le**, P.-L. Chen, and J. Hong, "Register driven means to control programming voltages", US Patent 6,304,487 (Issued on October 16, 2001).
32. J. Pawletko, **B. Q. Le**, P.-L. Chen, and J. Hong, "System for programming memory cells", US Patent 6,295,228 (Issued on September 25, 2001).
31. **B. Q. Le**, and P.-L. Chen, "Method and low-power circuits used to generate accurate boosted wordline voltage for flash memory core cells in read mode", US Patent 6,292,406 (Issued on September 18, 2001).
30. **B. Q. Le**, P.-L. Chen, and M. Van Buskirk, "Method and low-power circuits used to generate accurate drain voltage for flash memory core cells in read mode", US Patent 6,292,399 (Issued on September 18, 2001).
29. P.-L. Chen, and **B. Q. Le**, "Method and apparatus for continuously regulating a charge pump output voltage using a capacitor divider", US Patent 6,288,951 (Issued on September 11, 2001).
28. **B. Q. Le**, and P.-L. Chen, "Reduction of voltage stress across a gate oxide and across a junction within a high voltage transistor of an erasable memory device", US Patent 6,275,424 (Issued on August 14, 2001).

27. S. Hollmer, **B. Q. Le**, and P.-L. Chen, "Memory system having a program and erase voltage modifier", US Patent 6,269,025 (Issued on July 31, 2001).
26. P.-L. Chen, M. Van Buskirk, S. Hollmer, **B. Q. Le**, S. Kawamura, C.-Y. Hu, Y. Sun, S. Haddad, and C. Chang, "Dual source side polysilicon select gate structure and programming method utilizing single tunnel oxide for nand array flash memory", US Patent 6,266,275 (Issued on June 24, 2001).
25. **B. Q. Le**, P.-L. Chen, and S.C. Hollmer, "Capacitor for use in a capacitor divider that has a floating gate transistor as a corresponding capacitor", US Patent 6,262,469 (Issued on July 17, 2001).
24. J. Pawletko, **B. Q. Le**, J. Hong, and P.-L. Chen, "System for erasing a memory cell", US Patent 6,246,611 (Issued on June 12, 2001).
23. **B. Q. Le**, and P.-L. Chen, "Reduction of voltage stress across a gate oxide and across a junction within a high voltage transistor of an erasable memory device", US Patent 6,240,017 (Issued on May 29, 2001).
22. **B. Q. Le**, K. Kurihara, and P.-L. Chen, "Method to reduce capacitive loading in flash memory X-decoder for accurate voltage control at wordlines and select lines", US Patent 6,208,561 (Issued on March 27, 2001).
21. A. Yang, S. Hollmer, and **B. Q. Le**, "Precharging mechanism and method for NAND-based flash memory devices", US Patent 6,175,523 (Issued on January 16, 2001).
20. **B. Q. Le**, P.-L. Chen, and S. Hollmer, "Floating gate capacitor for use in voltage regulators", US Patent 6,137,153 (Issued on October 24, 2000).
19. **B. Q. Le**, P.-L. Chen, and S. Hollmer, "EEPROM decoder block having a p-well coupled to a charge pump for charging the p-well and method of programming with the EEPROM decoder block", US Patent 6,081,455 (Issued on June 27, 2000).
18. **B. Q. Le**, S.C. Hollmer, and P.-L. Chen, "Method of erasing floating gate capacitor used in voltage regulator", US Patent 6,072,275 (Issued on June 6, 2000).
17. **B. Q. Le**, P.-L. Chen, S. Hollmer, and A. Tan, "Methods and apparatus to perform high voltage electrical rule check of MOS circuit design", US Patent 6,055,366 (Issued on April 25, 2000).
16. S. Hollmer, C,-Y. Hu, **B. Q. Le**, P.-L. Chen, J. Su, R. Gutala, and C. Bill, "Erase verify scheme for NAND flash", US Patent 6,009,014 (Issued on December 28, 1999).
15. S. Hollmer, **B. Q. Le**, and P.-L. Chen, "Split voltage for NAND flash", US Patent 6,005,804 (Issued on December 21, 1999).
14. P.-L. Chen, M. Van Buskirk, S. Hollmer, **B. Q. Le**, S. Kawamura, C.-Y. Hu, Y. Sun, S. Haddad, and C. Chang, "Dual source side polysilicon select gate structure and programming method utilizing single tunnel oxide for NAND array flash memory" US Patent 5,999,452 (Issued on December 7, 1999).
13. P.-L. Chen, M. Chung , S. Hollmer, V. Leung, **B. Q. Le**, and M. Yano, "Scheme for page erase and erase verify in a non-volatile memory array", US Patent 5,995,417 (Issued on November 30, 1999).

12. P.-L. Chen, M. Van Buskirk, S. Hollmer, M. Chung, **B. Q. Le**, V. Leung, S. Kawamura, and M. Yano, "Bit line biasing method to eliminate program disturbance in a non-volatile memory device and memory device employing the same", US Patent 5,978,627 (Issued on November 2, 1999)
11. P.-L. Chen, S. Hollmer, **B. Q. Le**, and M. Chung, "Array VSS biasing for NAND array programming reliability, US patent 5,978,266 (Issued on November 2, 1999).
10. **B. Q. Le**, P.-L. Chen, and S. Hollmer, "Charge pump circuit architecture", US Patent 5,973,546 (Issued on October 26, 1999).

9. **B. Q. Le**, P.-L. Chen, and S. C. Hollmer, "Fast high voltage NMOS pass gate for integrated circuit with high voltage generator", US Patent 5,939,928 (Issued on August 17, 1999).
8. P.-L. Chen, M. Van Buskirk, S. C. Hollmer, **B. Q. Le**, S. Kawamura, C.-Y. Hu, Y. Sun, S. Haddad, and C. Chang, "Dual source side polysilicon select gate structure utilizing single tunnel oxide for NAND array flash memory", US Patent 5,912,489 (Issued on June 15, 1999).
6. **B. Q. Le**, P.-L. Chen, S. C. Hollmer, C.-Y. Hu, and N. Derhacobian, "High voltage NMOS pass gate having supply range, area, and speed advantages", US Patent 5,909,396 (Issued on June 1, 1999).
6. **B. Q. Le**, P.-L. Chen, S. C. Hollmer, S. Kawamura, M. S. Chung, V. C. Leung, and M. Yano, "High voltage NMOS pass gate for integrated circuit with high voltage generator and flash non-volatile memory device having the pass gate", US Patent 5,852,576 (Issued on December 22, 1998).
5. **B. Q. Le**, P.-L. Chen, S. C. Hollmer, C.-Y. Hu, and N. Derhacobian, "High voltage NMOS pass gate having supply range, area, and speed advantages", US Patent 5,844,840 (Issued on December 1, 1998).
4. **B. Q. Le**, S. Kawamura, P.-L. Chen, and S. Hollmer, "High-voltage CMOS level shifter", US Patent 5,821,800 (Issued on October 13, 1998).
3. **B. Q. Le**, P.-L. Chen, and S. Hollmer, "Charge pump circuit having non-uniform stage capacitance for providing increased rise time and reduced area", US Patent 5,818,288 (Issued on October 6, 1998).
2. **B. Q. Le**, P.-L. Chen, S. Hollmer, S. Kawamura, M. Chung, V. Leung, and M. Yano, "High voltage NMOS pass gate for integrated circuit with high voltage generator", US Patent 5,801,579 (Issued on September 1, 1998).
1. S. C. Hollmer, P.-L. Chen, and **B. Q. Le**, "Parallel page buffer verify or read of cells on a word line using a signal from a reference cell in a flash memory device", US Patent 5,638,326 (Issued on June 10, 1997).