HIU YUNG WONG

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Education

- **THE UNIVERSITY OF CALIFORNIA, BERKELEY (UCB)**
  Ph.D.: Electrical Engineering and Computer Science — July 2006
  Thesis: ***Advanced Gate Processes for Nanoscale CMOS***
  Advisor: Prof. Tsu-Jae King Liu
  Major: *Electronic Device Physics and Processing*
  Minor: *Integrated Circuits* (Internal), *Quantum Mechanics* (External)

- **THE CHINESE UNIVERSITY OF HONG KONG (CUHK)**
  M. Phil.: Computer Science and Engineering — July 2001
  Thesis: ***Matching Properties and Applications of Compatible Lateral Bipolar Transistors***
  Advisor: Prof. Philip Heng Wai Leong

  B.Eng. (First class honor): Computer Engineering — July 1999
  Minor: Business Administration
  Thesis: ***Solving Constraint Satisfactory Problems using FPGAs***
  Advisor: Prof. Philip Heng Wai Leong

Professional Experience

Program Director, MS Quantum Technology Program — **San Jose State University** — **2024-**

Associate Professor, Electrical Engineering — **San Jose State University** — **2022-**

Assistant Professor, Electrical Engineering — **San Jose State University** — **2018-2022**

- Machine learning to discover physical models and debug process/circuit
- Memory material characterization and simulation for leakage
- Compact model for neuromorphic simulation
- Calibration and simulation of novel WBG power device for electric vehicles and others
- Electrically variable gate length transistor for sub-5nm nodes
- Cryogenic calibration of CMOS devices for quantum computing interface
- Reliability modeling of IoT Devices

Visiting Scholar, TCAD Simulation, Prof. King-Liu's group — **UC Berkeley** — **2019-2020**

Senior Staff Applications Engineer — **Synopsys Inc.** — **2009 – 2018**

- **Reliability simulations on GaN defects and FinFET/nanowire NBTI**
- **Novel power device and reliability simulations/modeling (GaN, Ga2O3, Diamond)**
- **Expert/Champion on the following simulation tools**
  - SDevice, SProcess, SBand/Sub-band BTE, Monte Carlo Transport, NEGF, STT-RAM, ReRAM, Ab-initio to TCAD link
- **A strong relationship with customers and understanding of the state of the art technologies**
- **Technical know-how**
  - Delivered more than 20 technically successful TCAD simulation benchmarks on our customers' products including Si LDMOS, GaN devices, SiC IGBT, Avalanche Photo Diodes (APD), optoelectronics, ReRAM, HCI effects in SOI
- **Pioneer Machine Learning** in TCAD simulations and applications

MTS Integration Engineer — **Spansion (AMD/Fujitsu) Inc.** — **2006 – 2009**

- 45nm/32nm NOR flash memory technology process integration and development
- Designed and verified 45nm test chip test structures layout

- STI, bitline, poly gate and CoSi modules optimization and Si defect studies
- Periphery device development and integration including simulation and bench measurements

Internship **Cypress Semiconductor** **2004 – 2005**

- Designed and applied non-melt and melt excimer laser annealing experiments to 200mm integration lots to mitigate poly gate depletion
- Owned 200mm integration with various novel gate and source/drain engineering splits

6'' CMOS baseline Process Development Team Member **UCB Microfabrication Lab** **2002-2005**

- Performed full CMOS process flow and device simulations
- Performed bench characterizations: IV, CV, Oxide BV, mobility extraction, ring oscillator measurement

Services at SJSU

CSU:
2023 Spring CSU NSF CAREER mentor and seminar panelist

University:
Vice Chair, Academic Senate, May 2025 -
Member, VP for Administration & Finance/CFO Search Committee, 2025
Review Panelist: Industry-Sponsored Researcher Award 2024
Co-Chair, 2024 General Education (GE) Summer Workgroup
Chair, SJSU Senate Policy Committee, Curriculum and Research, Spring 2023 – Spring 2025
SJSU Academic Senator (10-EN-23, 11-EN-26) 2022- present
SJSU Senate Policy Committee, Curriculum and Research, 2022- 2025
Transformation 2030 Strategic Plan Working Groups (2024 -)
Senior Vice Provost Five-year Review Committee (2024)
Naming Committee, Spring 2023
Appeals Committee, Spring 2024

College of Engineering:
College Research Committee, College of Engineering, 2022- present
College Designated Graduate Advisor Committee, College of Engineering, 2023- present
Member, Strategic Plan Task Force, College of Engineering, 2022
College Assessment Committee, College of Engineering, 2018-2022
ESSC's Sophomore Success Program 2021
Associate Dean Search Committee, College of Engineering, 2021
Contributor, Strategic Plan, College of Engineering, 2019

Department of EE:
Faculty Search Committee 2024-2025
Lab director: Electronics Design II ENGR258 and Quantum Computing, Embedded Systems ENGR389
Scholarship Committee, 2023 - present
Graduate Program Coordinator, MS Quantum Technology Program, 2023 – present
Graduate Program Coordinator, MS Electrical Engineering Program, 2023 – present
Faculty Search Committee, 2022-2023 (opening closed)
Chair Review Committee, Electrical Engineering, 2021
Department Assessment Committee, Electrical Engineering, 2019-2022
Department Graduate Curriculum Committee, Electrical Engineering, 2019- present
Department Undergraduate Curriculum Committee, Electrical Engineering, 2019- present

Student Service:
Advisor to Society of Quantum Engineers at SJSU, Fall, 2023 - present
Advisor to SJSU IEEE Student Chapter, Spring 2023 - present

Professional Activities

Editor:

- Editor, IEEE Journal of the Electron Devices Society (JEDS), 2025-
- Associate Editor, IEEE Access (2020 - 2022)
- Guest Editor, Micromachines, special issue on "Novel Ultra Wide Bandgap Power Devices and Materials", 2020
- Guest Editor, Journal of Vacuum Science and Technology B, special issue on "Reliability and Stress-related Phenomena in Nano and Microelectronics", 2020

Conference Organizer:

- Co-Chair and Technical Chair, International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) 2024
- Technical Program Committee, IEEE Workshop on Quantum Computing: Devices, Cryogenic Electronics and Packaging, 2023
- Executive Committee, 5th IEEE International Flexible Electronics Technology Conference (IFETC) 2023
- Technical Program Committee (TPC), International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) (20,21,23)
- Technical Program Committee (TPC), 2022 International Conference on Computer-Aided Design (ICCAD) (2022)
- Vice-Chair, 16th International Conference on Reliability and Stress-related Phenomena in Nano and Microelectronics (IRSP19)
- Member of International Program Committees for The IASTED International Conference on Control and Optimization of Renewable Energy Systems CORES 2019
- Workshop Moderator, "Circuit Reliability: Advanced nodes concerns and CAD tools flows" 2018 IEEE International Reliability Physics Symposium (IRPS)

Senior Member of the Institute of Electrical and Electronics Engineers (IEEE)

Member, Technical Working Group on Emerging Research Devices, IEEE, Heterogeneous Integration Roadmap (HIR)

IEEE EDS Educational Activities Committees (2025)

IEEE EDS Community Engagement Ad Hoc Committee (2025)

IEEE EDS-SCV/SF Chapter Officer

- Chair (2023-2024, interim 2022)
- Treasurer (2019-2022)
- Secretary (2018-2019)
- Publicity Chair (2025)
- Executive committee board (2018-)

Reviewer:
Grants/Awards:
2022 NASA Early Career Faculty Review Panel
2022 NSF Research Traineeship (NRT) Program Review Panel
2019 NASA Fellowship (Program Officer, Brenda Collins)

Journals: Scientific Reports, IEEE Electron Device Letters (EDL), Applied Physics Letters (APL), IEEE Transactions on Circuits and Systems II (TCAS-II), IEEE Transaction on Electron Devices (TED), IEEE Journal of Electron Devices Society (J-EDS), IEEE Access, IEEE Transactions on Quantum Engineering, IEEE Transactions on Semiconductor Manufacturing, IEEE Transaction on Nanotechnology (TNANO), Diamond & Related Materials (DRM), IET Electronics Letters, IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), ECS Journal of Solid State Science and Technology, IET Circuits, Devices & Systems, Journal of the Electrochemical Society, Electrochemical and Solid-State Letters, Solid-State Electronics, Power Electronic Devices and Components.

Outreach:

- Organizer and speaker: QuDIT Testbed Workshop – the 'Real World Quantum Computing @ LLNL' 2022, 2023, 2024, 2025
- Summer class by Silicon Tech Academy, "Intro to Python Programming - with Machine Learning & Quantum Computing Applications". Two-week hands-on class for 8^{th}-9^{th} grade students (free for social-economically disadvantaged students). 2022, 2023, 2025
- Judge**:** The Synopsys Championship (the Santa Clara County science fair for students in grades 6-12), Sciencepalooza! (for students in grades 9-12 in East San José)
- Summer Class: "Introduction to Python Programming and Machine Learning" 6/30/2020-7/1/2020 for Downtown College Prep high school students.

Grants

2018 Fall – present: US$5M awarded (US$2.4M to Wong's Lab)

Extramural:

G1. **Sandia National Laboratories (SNL),** GAA-FET SRAM Radiation Hardness Projection, US$ 75,000, *PI* (100%) (2024-2025)
G2. **National Science Foundation**, Collaborative Research: Elements: Empowering Semiconductor Device Research and Education through Integrated Machine Learning Models and Database, US$216K, **PI** (100%) 2410694 (2024-2027)
G3. **National Science Foundation**, FuSe2 Topic 2: Heterogenous Integration of Wide-Bandgap Microelectronics and Power Electronics for Efficient Power Delivery to AI Processors in Data Centers, US$1,800K, **co-PI** (16.7%) 2424859 (2024-2027)
G4. **Atomera Inc,** Cryogenic Characterization and Modeling of MST Devices and Analog Circuits Augmented with TCAD-enabled Machine Learning, US$ 100,195, *PI* (100%) (2024-2025)
G5. **Samsung Inc,** Cryogenic MOSFET Mobility Extraction and Modeling, US$75,000, *PI* (100%) (2023)
G6. **Atomera Inc,** Cryogenic Characterization of MST Devices, US$50,052, *PI* (100%) (2022)
G7. **Atomera Inc,** Circuit Simulation, Carrier Transport Physics Characterization, and BTI Reliability Modeling of MST, US$11,751, *PI* (100%) (2022)
G8. **Atomera Inc,** Circuit Simulation, Carrier Transport Physics Characterization, and BTI Reliability Modeling of MST, US$50K, *PI* (100%) (2021)
G9. **National Science Foundation**, CAREER: Understanding and Modeling of Cryogenic Semiconductor Device Physics down to 4.2K, US$500K, **PI** (100%) 2046220 (2021-2026)
G10. **National Science Foundation**, FMSG: Cyber: Cybermanufacturing of Wide-Bandgap Semiconductor Devices Enabled by Simulation Augmented Machine Learning, US$500K, **co-PI** (40%) 2134374 (2021-2023)
G11. **National Science Foundation**, Collaborative Research: NRT-QL: A Program for Training a Quantum Workforce, US$739K, **co-PI** (33%) 2125906 (2021-2026)
G12. **National Science Foundation**, RET site: Multidisciplinary Teacher Research Experience in Engineering (M-TREE), US$600K, **Senior Personnel** (3.3%) (2021-2024)
G13. **Applied Materials Inc,** Power Device Simulation and Optimization, US$65K, **PI** (100%) (2021-2022)
G14. **Synopsys Inc,** Materials Modeling Research Project, US$15K, **PI** (100%) (2020-2021)
G15. **Atomera Inc,** Modeling and Simulation of MST, US$75K, *PI* (100%) (2020)
G16. **Department of Energy, PowerAmerica,** Development of Low-Cost Graduate Course with Virtual Fab and Hands-on Circuit Lab Experience to Prepare Students to Work in the SiC Industry in Silicon Valley, US$50K, **PI** (50%) (2019-2020)
G17. **NASA,** Chip Design for Self-Healing Electronics, US$ 50K, **PI** (100%) (2019-2020)

G18. **Department of Defense, Naval Surface Warfare Center Crane Division**, Radiation Hardness Projection and Optimization of sub-10nm Technology Node SRAM through Design-Technology-Co-Optimization (DTCO) Simulations, US$ 26K, **PI** (100%) (2019)
G19. **Atomera Inc,** Modeling and Simulation of MST, US$27.5K, **PI** (100%) (2019)
G20. **Synopsys Inc,** Materials Modeling Research Project, US$30K, **PI** (100%) (2019-2020)
G21. **Atomera Inc,** CMOS applications of MST film using TCAD, US$25K, **PI** (100%) (2019)

Internal (SJSU):
G22. **2024 SJSU RSCA Equipment Grant**, Customized Superconducting Quantum Chip Design and Testing, US$35,000, **PI** (33.4%), (2024-2025)
G23. **2024 SJSU RSCA Seed Grant**, Optimization of Variational Quantum Linear Solver on Quantum Computer, US$7,500, **PI** (100%), (2024-2025)
G24. **SJSU, AMDT Endowment Funding,** US$300K, **PI** (100%) (2022-2023)
G25. **SJSU, The Level-Up Grant,** Development of Cryogenic Transistor Model for Quantum Computing Peripherals, US$9,350, **PI** (100%) (2020-2021)
G26. **SJSU COE,** Design Technology Co-Optimization (DTCO) Framework for Neuromorphic Computing: from Device to System, US $100,000, **PI** (34%) (2019-2020)

Patents

P1. **Hiu Yung Wong**. Variable Channel Doping in Vertical Transistor. US Provisional Patent App. US 63/223,459, 2021.
P2. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Machine Learning for Optimizing Setups for Accurate, Speedy and Robust TCAD Simulations. U.S. Patent No. 11,348,017. Issued May 17, 2022.
P3. **Hiu Yung Wong** and Rimvydas Mickevicius. Using Threading Dislocations in GaN/Si System to generate Physical Unclonable Function (PUF). U.S. Patent No. 11,152,313. Issued October 5, 2021.
P4. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Constricted Junction-less FinFET/ Nanowire/ Nanosheet with normally-off VTH, high ION and low leakage. U.S. Patent No. 10,777,638. Issued September 15, 2020.
P5. **Hiu Yung Wong** and Rimvydas Mickevicius. A new local Band-to-Band Tunneling (BTBT) model for more accurate and speedy TCAD simulations. U.S. Patent No. 10,769,339. Issued September 8, 2020.
P6. **Hiu Yung Wong**, Victor Moroz, and Qiang Lu. Anti-punch-through implant or its extension/variations as heater for on-chip self-heating and self-annealing. U.S. Patent No. 10,699,914. Issued June 30, 2020.
P7. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Normally-off Gallium Oxide Field-Effect Transistor. U.S. Patent No. 10,644,107. Issued May 5, 2020.
P8. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Monolithically Integrated III-Nitride Cascode Circuit for High Voltage Application. U.S. Patent No. 10,403,625. Issued September 3, 2019.
P9. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Heterojunction Field Effect Transistor Device with Serially Connected Enhancement Mode and Depletion Mode Gate Regions. U.S. Patent No. 10,128,232. Issued November 13, 2018.
P10. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Tined gate to control threshold voltage in a device formed of materials having piezoelectric properties. U.S. Patent No. 9,837,523. filed 13 Apr 2016 and issued 5 Dec 2017.
P11. Eunha Kim, Wen Yu, Minh-Van Ngo, Kyunghoon Min and **Hiu Yung Wong**. Forming metal-semiconductor films having different thicknesses within different regions of an electronic device. US Patent 7,880,221, filed 19 Dec 2008, and issued 1 Feb 2011.

P12. Eunha Kim, Wen Yu, Minh-Van Ngo, Kyunghoon Min and **Hiu Yung Wong**. Forming metal-semiconductor films having different thicknesses within different regions of an electronic device. US Patent 7,482,217, filed 3 Dec 2007, and issued 27 Jan 2009.

Awards

- Recognized in SJSU "Annual Author and Artist Celebration 2024" for the textbook published (Introduction to Quantum Computing, 2nd edition), 2025.
- 2024 Nominee by SJSU President for CSU The Wang Family Excellence Award - "Outstanding Faculty Innovator in Student Success"
- Emeritus and Retired Faculty Association Faculty Research and Creative Activity Award, 2024-2025
- 2023 Industry Sponsored Research Award
- Recognized in SJSU "Annual Author and Artist Celebration 2022" for the textbook published (Introduction to Quantum Computing), 2023.
- 2022 Curtis W. McGraw Research Award (ASEE Engineering Research Council)
- AMDT Endowed Chair Professor 2022
- NSF CAREER Award, 2021
- The 2021 Newnan Brothers Award for Faculty Excellence, "demonstrate excellence in some combination of teaching, service to students, and/or research".
- San Jose State University Grants Academy award, 2019
- Synopsys Outstanding Contribution to Results Award (For supporting foundry FinFET simulation), 2013
- Synopsys Outstanding Contribution to Results Award (For leading power device simulation), 2010
- Synopsys Excellence Award (1 out of every ~500 employees), 2010
- Sir Edward Youde Memorial Fellowships for Overseas Studies, 2001

Books

B1. **Hiu Yung Wong,** *Introduction to Quantum Computing: From a Layperson to a Programmer in 30 Steps*. Switzerland: Springer International Publishing, First Edition: 2022. https://doi.org/10.1007/978-3-030-98339-0. ISBN-10: 3030983382. Second Edition: 2023, https://doi.org/10.1007/978-3-031-36985-8. ISBN: 978-3-031-36984-1

B2. **Hiu Yung Wong,** *Quantum Computing Architecture and Hardware for Engineers - Step by Step*. Switzerland: Springer International Publishing, 2025. https://doi.org/10.1007/978-3-031-78219-0

Book Chapter

C1. Chatterjee, B., Shoemaker, D., **Wong, H.**, and Choi, S, "AlGaN/GaN HEMT device physics and electrothermal modeling," Chapter 6 in Thermal Management of Gallium Nitride Electronics, Marko J. Tadjer and Travis J. Anderson, Editors, Woodhead Publishing, 2022.

Peer-Reviewed Journal Papers (+: Supervised Students)

J1. **Edric Khai Jieh Ong**+, Le Minh Long Nguyen+, Matthew Eng+, Yuhao Zhang, and **Hiu Yung Wong**, "Ga2O3 TCAD Mobility Parameter Calibration using Simulation Augmented Machine Learning with Physics Informed Neural Network," **submitted**.

J2. Daniel Gutierrez, Pranay Doshi, **Hiu Yung Wong**, Dennis Nordlund and Ram P. Gandhiraman, "Printed graphene and its composite with copper for electromagnetic interference shielding applications," *Nanotechnology* 2024 Jan 10;35(13). doi: 10.1088/1361-6528/ad12e9.

J3. Y. Wang, M. Porter, M. Xiao, A. Lu+, N. Yee+, I. Kravchenko, B. Srijanto, K. Cheng, **H. Y. Wong**, and Y. Zhang, "Implanted Guard Ring Edge Termination With Avalanche Capability for Vertical GaN Devices," in IEEE Transactions on Electron Devices, doi: 10.1109/TED.2023.3321010.

J4. **Tom Jiao+,** Edwin Antunez+**, and Hiu Yung Wong**, "Study of Cryogenic MOSFET Sub-Threshold Swing Using Ab Initio Calculation," in *IEEE Electron Device Letters*, vol. 44, no. 10, pp. 1604-1607, Oct. 2023, doi: 10.1109/LED.2023.3310511.

J5. **A. Zaman**+, Hector Morrell+, and **Hiu Yung Wong**, "A Step-by-Step HHL Algorithm Walkthrough to Enhance Understanding of Critical Quantum Computing Concepts," in IEEE Access, 2023. 10.1109/ACCESS.2023.3297658.

J6. **Hiu Yung Wong**, "TCAD Simulation Models, Parameters, and Methodologies for beta-Ga2O3 Power Devices," ECS Journal of Solid State Science and Technology, 12 055002, 2023. DOI 10.1149/2162-8777/accfbe.

J7. Pranay Doshi, **Hiu Yung Wong**, Daniel H. Gutierrez, Arlene Lopez, Dennis Nordlund and Ram Prasad Gandhiraman, "Printing of electromagnetic interference shielding materials," 2023 Flex. Print. Electron. 8 025003. DOI 10.1088/2058-8585/acc879

J8. **Hiu Yung Wong**, Prabjot Dhillon+, Kristin Beck, and Yaniv Jacob Rosen, "A Simulation Methodology for Superconducting Qubit Readout Fidelity," Solid-State Electronics, Volume 201, March 2023, 108582. https://doi.org/10.1016/j.sse.2022.108582.

J9. Ravi Tiwari, Meng Duan, Mohit Bajaj, Denis Dolgos, Lee Smith, **Hiu Yung Wong**, and Souvik Mahapatra, "A Physics-based TCAD Framework for NBTI," Solid-State Electronics, https://doi.org/10.1016/j.sse.2022.108573.

J10. **Albert Lu**+, Adam Elwailly+, Yuhao Zhang and **Hiu Yung Wong**, "Study of Vertical Ga2O3 FinFET Short Circuit Ruggedness using Robust TCAD Simulation," ECS J. Solid State Sci. Technol, 2022. https://doi.org/10.1149/2162-8777/ac9e73

J11. **Albert Lu+,** Jordan Marshall+, Yifan Wang, Ming Xiao, Yuhao Zhang, and **Hiu Yung Wong**, "Vertical GaN Diode BV Maximization through Rapid TCAD Simulation and ML-enabled Surrogate Model," Solid-State Electronics, Volume 198, December 2022, 108468, https://doi.org/10.1016/j.sse.2022.108468.

J12. **V. Eranki+**, N. Yee and **H. Y. Wong**, "Out-of-Training-Range Synthetic FinFET and Inverter Data Generation Using a Modified Generative Adversarial Network," in IEEE Electron Device Letters, vol. 43, no. 11, pp. 1810-1813, Nov. 2022, doi: 10.1109/LED.2022.3207784.

J13. **Tom Jiao**+ and **Hiu Yung Wong**, "Robust Cryogenic Ab-initio Quantum Transport Simulation for LG=10nm Nanowire," Solid-State Electronics, Volume 197, 2022, 108440, doi.org/10.1016/j.sse.2022.108440.

J14. **H. Y. Wong,** "Ab Initio Study of HfO2/Ti Interface VO/Oi Frenkel Pair Formation Barrier and VO Interaction With Filament," in IEEE Transactions on Electron Devices, vol. 69, no. 9, pp. 5130-5137, Sept. 2022, doi: 10.1109/TED.2022.3188227.

J15. **P. Quibuyen**+, T. Jiao+, and **H. Y. Wong**, "A Software-Circuit-Device Co-Optimization Framework for Neuromorphic Inference Circuits," in IEEE Access, vol. 10, pp. 41078-41086, 2022, doi: 10.1109/ACCESS.2022.3167709.

J16. **Prabjot Dhillon**+ and **Hiu Yung Wong**, "A Wide Temperature Range Unified Undoped Bulk Silicon Electron and Hole Mobility Model," in *IEEE Transactions on Electron Devices*, doi: 10.1109/TED.2022.3152471. (2022)

J17. **Thomas Lu**+, Varada Kanchi+, Kashyap Mehta+, Sagar Oza+, Tin Ho+, and **Hiu Yung Wong**, "Rapid MOSFET Contact Resistance Extraction from Circuit using SPICE Augmented Machine Learning without Feature Extraction," in *IEEE Transactions on Electron Devices*, vol. 68, no. 12, pp. 6026-6032, Dec. 2021, doi: 10.1109/TED.2021.3123092.

J18. J. Lundh, D. Shoemaker, A. G. Birdwell, J. D. Weil, L. M. De La Cruz, P. B. Shah, K. G. Crawford, T. G. Ivanov, **H. Y. Wong**, and S. Choi, "Thermal performance of diamond field-effect transistors," Appl. Phys. Lett. 119, 143502 (2021); https://doi.org/10.1063/5.0061948.

J19. **Harsaroop Dhillon+,** Kashyap Mehta+, Ming Xiao, Boyan Wang, Yuhao Zhang, and **Hiu Yung Wong**, "TCAD-Augmented Machine Learning with and without Domain Expertise," in IEEE Transactions on Electron Devices, vol. 68, no. 11, pp. 5498-5503, Nov. 2021, doi: 10.1109/TED.2021.3073378.

J20. **A. Elwailly**+, J. Saltin+, M. J. Gadlage and **H. Y. Wong**, "Radiation Hardness Study of LG = 20 nm FinFET and Nanowire SRAM Through TCAD Simulation," in IEEE Transactions on Electron Devices, vol. 68, no. 5, pp. 2289-2294, May 2021, doi: 10.1109/TED.2021.3067855.

J21. **K. Mehta**[+] and **Hiu Yung Wong**, "Prediction of FinFET Current-Voltage and Capacitance-Voltage Curves Using Machine Learning With Autoencoder," in *IEEE Electron Device Letters*, vol. 42, no. 2, pp. 136-139, Feb. 2021, doi: 10.1109/LED.2020.3045064.

J22. Fei Ding, **Hiu-Yung Wong** and Tsu-Jae King Liu, "Design optimization of Sub-5nm Node Nanosheet Field Effect Transistors to Minimize Self-Heating Effects," Journal of Vacuum Science and Technology B, B 39, 013201 (2021); https://doi.org/10.1116/6.0000675. **(Editor's Pick)**

J23. **Hiu Yung Wong**, Ming Xiao, Boyan Wang, Yan Ka Chiu[+], Xiaodong Yan, Jiahui Ma, Kohei Sasaki, Han Wang, and Yuhao Zhang, "TCAD-Machine Learning Framework for Device Variation and Operating Temperature Analysis With Experimental Demonstration," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 992-1000, 2020, doi: 10.1109/JEDS.2020.3024669.

J24. Uma Sharma, Meng Duan, Himanshu Diwakar, Karansingh Thakor, **Hiu Yung Wong**, Steve Motzny, Denis Dolgos and Souvik Mahapatra, "TCAD Framework for HCD Kinetics in Low VD Devices Spanning Full VG/VD Space," in *IEEE Transactions on Electron Devices*, doi: 10.1109/TED.2020.3021360.

J25. Cyril Buttaya, **Hiu-Yung Wong**, Boyan Wang, Ming Xiao, Christina DiMarino and Yuhao Zhang, "Surge Current Capability of Ultra-Wide-Bandgap Ga2O3 Schottky Diodes," Microelectronics Reliability, Volume 114, November 2020, 113743. 10.1016/j.microrel.2020.113743.

J26. **K. Mehta**[+], S. S. Raju[+], M. Xiao, B. Wang, Y. Zhang and **H. Y. Wong**, "Improvement of TCAD Augmented Machine Learning Using Autoencoder for Semiconductor Variation Identification and Inverse Design," in IEEE Access, vol. 8, pp. 143519-143529, 2020, doi: 10.1109/ACCESS.2020.3014470.

J27. **J. Saltin**[+], N. C. Dao, P. H. W. Leong and **H. Y. Wong**, "Energy Filtering Effect at Source Contact on Ultra-Scaled MOSFETs," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 662-667, 2020, doi: 10.1109/JEDS.2020.2981251.

J28. **Hiu Yung Wong** and Armand Tenkeu[+], "Advanced TCAD Simulation and Calibration of Gallium Oxide Vertical Transistor," ECS Journal of Solid State Science and Technology 9 (3), 035003, 2020.

J29. **Hiu-Yung Wong**, Denis Dolgos, Lee Smith, Rimvydas V. Mickevicius, "Modified Hurkx Band-to-Band-Tunneling Model for Accurate and Robust TCAD Simulations," Microelectronics Reliability, Volume 104, January 2020, 113552.

J30. Boyan Wang, Ming Xiao, Xiaodong Yan, **Hiu Yung Wong**, Jiahui Ma, Kohei Sasaki, Han Wang, and Yuhao Zhang, "High-voltage vertical Ga2O3 power rectifiers operational at high temperatures up to 600 K", Appl. Phys. Lett. 115, 263503 (2019); https://doi.org/10.1063/1.5132818.

J31. Ravi Tiwari, Narendra Parihar, Karansingh Thakor, **Hiu Yung Wong,** Steve Motzny, Munkang Choi, Victor Moroz and Souvik Mahapatra, "A 3-D TCAD Framework for NBTI, Part-I: Implementation Details and FinFET Channel Material Impact, in IEEE Transactions on Electron Devices, vol. 66, no. 5, pp. 2086-2092, May 2019.

J32. Ravi Tiwari, Narendra Parihar, Karansingh Thakor, **Hiu Yung Wong,** Steve Motzny, Munkang Choi, Victor Moroz and Souvik Mahapatra, "A 3-D TCAD Framework for NBTI, Part-II: Impact of Mechanical Strain, Quantum Effects and FinFET Dimension Scaling, in IEEE Transactions on Electron Devices, vol. 66, no. 5, pp. 2093-2099, May 2019.

J33. **Hiu Yung Wong,** Nelson Braga and R. V. Mickevicius, "Enhancement Mode Recessed Gate and Cascode Gate Junctionless Nanowire with Low Leakage and High Drive Current," in IEEE Transactions on Electron Devices, vol. 65, no. 9, pp. 4004-4008, Sept. 2018.

J34. P. Pfäfflia, **H.Y. Wong**, X. Xu, L. Silvestria, X.W. Lin, T. Yang, R. Tiwari, S. Mahapatra, S. Motzny, V. Moroz and Terry Ma, "TCAD Modeling for Reliability," Microelectronics Reliability, Volumes 88–90, September 2018, Pages 1083-1089.

J35. **Hiu Yung Wong,** Nelson Braga and R. V. Mickevicius, "Prediction of highly scaled hydrogen-terminated diamond MISFET performance based on calibrated TCAD simulation," Diamond and Related Materials, Volume 80, November 2017, Pages 14-17.

J36. **Hiu Yung Wong**, Nelson Braga, R. V. Mickevicius, " Normally-off GaN HFET based on Layout and Stress Engineering ", IEEE Electron Device Letters, 37 (12), 1621-1624.

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C77. **H.-Y. Wong,** H. Takeuchi, T.-J. King, M. Ameen, and A. Agarwal, "Reduced poly-Si gate depletion effect by pulsed excimer laser annealing," presented at the 205th ECS Meeting, Advanced Short-Time Thermal Processing for Si-Based CMOS Devices II Symposium (San Antonio, TX, USA), May 2004. **(INVITED PAPER)**

C78. H. Takeuchi, **H. Y. Wong**, D. Ha, and T.-J. King, "Impact of oxygen vacancies on high-k gate dielectric engineering," International Electron Devices Meeting Technical Digest, pp. 829-832, 2004.

C79. **H. Y. Wong**, K. Shin, and M. Chan, "The Gate Misalignment Effects of the Sub-threshold Characteristics of sub-100nm DG-MOSFETs", 2002 IEEE Hong Kong Electron Devices Meeting Proceedings, pp. 91-94, June 22, 2002, Hong Kong

C80. Neil N. H. Ching, **Hiu Yung Wong**, Wen J. Li, and Philip H. W. Leong, "A laser-micromachined vibrational to electrical power transducer for wireless sensing systems", 11th International Conference on Solid-State Sensors and Actuators, (Transducers '01 / Eurosensors XV), Munich, Germany, June 2001.

C81. Neil N. H. Ching, Gordon M. H. Chan, Wen J. Li, **Hiu Yung Wong**, and Philip H. W. Leong, "PCB-integrated Micro-generator Arrays for Wireless Systems", International Symposium on Smart Structures and Microsystems, Oct. 19-21, 2000, Hong Kong.

C82. Wen J. Li, Philip H. W. Leong, Terry C. H. Hong, **Hiu Yung Wong**, and Gordon M. H. Chan, "Infrared Signal Transmission by a Laser-micromachined vibration-induced power generator", Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems, August 8-11, pp. 236-239, 2000

C83. **H. Y. Wong**, W. S. Yuen, K. H. Lee and P. H. W. Leong, "A Runtime Reconfigurable Implementation of the GSAT Algorithm", the Proceedings of the Ninth International Workshop on Field Programmable Logic and Applications (FPL'99) Glasgow, UK, pp. 526-531, 1999

Invited Workshops and Tutorials:

W1. **Hiu Yung Wong** and Imran Bashir, Tutorial: Electrical Circuit and Qubit Interactions in Silicon and Superconducting Qubits. IEEE Quantum Week 2025.

W2. **Hiu Yung Wong,** (Ultra) Wide Bandgap Material Process and Device TCAD Simulation Methodologies, the 11th Annual IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2024), 2024.

W3. **Hiu Yung Wong** and Imran Bashir, Tutorial: Electrical Circuit and Qubit Interactions in Silicon and Superconducting Qubits. IEEE Quantum Week 2024.

W4. **Hiu Yung Wong,** Tutorial on Superconducting Qubit Design with Qiskit Metal and HFSS, Qubit Design Spring 2024, CosmiQ group, FermiLab, 2024.

W5. **Hiu Yung Wong,** Tutorial: Introduction to Quantum Computing: from Algorithm to Hardware. The IEEE Custom Integrated Circuits Conference (CICC) 2024.

W6. **Hiu Yung Wong,** Workshop: Quantum Computing and Simulation**,** SISPAD 2023

W7. **Hiu Yung Wong,** Tutorial: Introduction to Quantum Computing: from Algorithm to Hardware. IEEE Quantum Week 2023.

W8. **Hiu Yung Wong,** Tutorial: Introduction to Quantum Computing: from Algorithm to Hardware. ISQED conference 2023

W9. **Hiu Yung Wong,** Workshop 1: Combination of TCAD and Machine Learning**,** SISPAD 2020.

W10. **Hiu Yung Wong,** (Ultra) Wide Bandgap Material Process and Device TCAD Simulation Methodologies, WiPDA-Asia, 2020

Panelist

I1. Cryogenic Electronics: Powering the Next Frontier in AI and Computing, the 26th International Symposium on Quality Electronic Design, ISQED conference 2025, San Francisco.

Invited Presentations

I1. **Hiu Yung Wong**, "Electrical Circuit and Qubit Interactions in Superconducting Qubit", IIT Kharagpur, YouTube Live, June 2025 (60 attendees) (https://www.youtube.com/live/QpPw-ZSR0jY)

I2. **Hiu Yung Wong**, "Electrical Circuit and Qubit Interactions in Superconducting Qubit", Samsung Forum, Samsung, San Jose, May 2025 (120 attendees)

I3. **Hiu Yung Wong**, "Introduction to Quantum Computing: From Algorithm to Hardware", Tesla Inc., Palo Alto, May 2025. (40 attendees)

I4. **Hiu Yung Wong**, "An Overview of Quantum Computing Hardware", Ansys Inc., November 2024. (20 attendees)

I5. **Hiu Yung Wong**, "Introduction to Quantum Computing", Evergreen Valley High School, San Jose, Sept. 2024. (30 attendees)

I6. **Hiu Yung Wong**, "Simulation-Augmented Machine Learning for Semiconductor Physics and Defect Discovery", Ansys Inc., February 2024. (20 attendees)

I7. **Hiu Yung Wong**, "Introduction to Quantum Computing – Basics, Hardware, and Simulation", Samsung Forum, Samsung, San Jose, February 2024. (222 attendees)

I8. **Hiu Yung Wong**, "Introduction to Quantum Computing: From Algorithm to Hardware", National Cheng Kung University, November 2023. (30 attendees)

I9. **Hiu Yung Wong**, "Introduction to Quantum Computing: From Algorithm to Hardware", Asia University, October 2023. (40 attendees)

I10. **Hiu Yung Wong**, "Simulation-Augmented Machine Learning for Semiconductor Physics", Washington DC Quantum Computing Meetup, August 2023. (50 attendees + 15 live stream)

I11. **Hiu Yung Wong**, "Introduction to Quantum Computing", IEEE SUST Student Branch, Bangladesh, June 2023. (30 attendees)

I12. **Hiu Yung Wong**, "Introduction to Quantum Hardware", 25th New Frontiers in Computing (NFIC) 2023 co-organized by NATEA and IEEE-Computer Society Santa Clara Valley, May 2023.

I13. **Hiu Yung Wong**, "Introduction to Quantum Computing: from Algorithm to Hardware", Washington DC Quantum Computing Meetup, April 2023. (100 attendees)

I14. **Hiu Yung Wong**, "Introduction to Quantum Computing", Lynbrook High School, San Jose, March 2023. (20 attendees)

I15. **Hiu Yung Wong**, "Cryogenic Semiconductor and Quantum Computing," at SJSU RSCA in Five: Faculty Short Talks on Semiconductors and Quantum Technologies, March 2023.

I16. **Hiu Yung Wong**, "Understanding Cryogenic Semiconductor Devices", CSU Exemplars in Physics, Oct. 2022

I17. **Hiu Yung Wong**, "Introduction to Quantum Computing", Synopsys, Inc., Mountain View, CA, September, 2022. (40 attendees)

I18. **Hiu Yung Wong**, "Introduction to Quantum Computing", Zen4Quantum, August, 2022. (40 attendees)

I19. **Bay Area Semiconductor Work Force Development Mini-Workshop**, August. 2022.

I20. **Hiu Yung Wong**, "Introduction to Quantum Computing", eBay, Inc., San Jose, CA, August. 2022. (30 attendees)

I21. **Hiu Yung Wong**, "A Beginner's Guide to Quantum Computing Webinar", FormFactor, Inc, Milpitas, CA, August. 2022. (>300 attendees)

I22. **Hiu Yung Wong**, "Introduction to Quantum Computing", Fujitsu Research of America, Sunnyvale, CA, May, 2022. (30 attendeeds)

I23. **Hiu Yung Wong**, "TCAD/SPICE-Augmented Machine Learning for Defect and Variation Study", IEEE-EDS Santa Clara Valley/San Francisco Chapter October Seminar, 2021.

I24. **Hiu Yung Wong**, "Simulation Augmented Machine Learning," at SJSU RSCA in Five: Faculty Short Talks on AI, Machine Learning, and Ethics, March 2021. (online)

I25. **Hiu Yung Wong**, Nelson Braga, and R. V. Mickevicius, TCAD modeling of hydrogen-terminated diamond FET for RF Applications, Mat Science 2020, San Francisco, CA, November 5-7, 2020. (online)

I26. **Hiu Yung Wong**, "TCAD Augmented Machine Learning", Micron, Inc., Boise, ID, Oct. 2020. (online)

I27. **Hiu Yung Wong**, "TCAD to SPICE: MST RF Simulation as an Example", Atomera, Inc., Saratoga, CA, Sept. 2020. (online)

I28. **Hiu Yung Wong**, "TCAD Seminar: Using Machine Learning in TCAD", Synopsys, Inc., Mountain View, CA, Aug. 2020. (online)

I29. **Hiu Yung Wong**, Modeling, Calibration and Simulation of Ga2O3 Vertical Diode and FinFET in TCAD, Workshop on Compound Semiconductor Materials and Devices WOCSEMMAD, Feb., 2020.

I30. **Hiu Yung Wong**, "TCAD Augmented Machine Learning for Semiconductor Device Failure Troubleshooting and Reverse Engineering", Silvaco, Inc., Santa Clara, CA, Oct 2019.

I31. **Hiu Yung Wong**, "Research at M-PAC lab", at SJSU Science and Engineering Tapas talks, 2019.

I32. **Hiu Yung Wong** and Johan Saltin[+], TCAD Simulation of Novel Gallium Oxide Power Device with High On/Off Ratio, Workshop on Compound Semiconductor Materials and Devices WOCSEMMAD, 2019.

I33. Rake-Gate AlGaN/GaN normally off HEMTs, Workshop on Compound Semiconductor Materials and Devices WOCSEMMAD, 2018.

I34. **Hiu Yung Wong**, "Selected TCAD Topics on More Moore and More than Moore", Seminar Talk in Department of Electronic Engineering, Chinese University of Hong Kong, Hong Kong, 2017.

I35. Low RC-constant Perforated-Channel HFET, Workshop on Compound Semiconductor Materials and Devices WOCSEMMAD, 2014,

I36. **Hiu Yung Wong,** "Elimination of Poly-Si Gate Depletion for Sub-65nm CMOS Technologies by Excimer Laser Annealing", West Coast Junction Technology Group Meeting, Sunnyvale, CA, 2005.

I37. **Hiu Yung Wong**, Laser Annealing Technology, AMD, Sunnyvale, CA, 2005.

Media:

M1. 2024: SJSU News Center: SJSU Awarded $4M in Federal Funding for STEM Research
https://blogs.sjsu.edu/newsroom/2024/sjsu-awarded-4m-in-federal-funding-for-stem-research/

M2. 2024: Media Alert: Atomera to Present Joint Paper with Soitec and San Jose State University on Advanced RF Technologies at 8th IEEE Electronic Devices Technology and Manufacturing (EDTM) Conference 2024
https://www.nasdaq.com/press-release/media-alert:-atomera-to-present-joint-paper-with-soitec-and-san-jose-state-university

M3. 2024: SJSU News Center: Second Annual SJSU Research Week to Celebrate and Highlight Public-Impact Research
https://blogs.sjsu.edu/newsroom/2024/second-annual-sjsu-research-week-to-celebrate-and-highlight-public-impact-research/

M4. 2024: SJSU News Center: A Quantum Leap into New Technology
https://blogs.sjsu.edu/newsroom/2024/a-quantum-leap-into-new-technology/

M5. 2023: Media Alert: Atomera to Present at SISPAD 2023
https://finance.yahoo.com/news/media-alert-atomera-present-sispad-210000756.html

M6. 2023: The Central News Agency (CNA): 矽谷科學家：量子電腦有望實現通用人工智慧
https://www.cna.com.tw/news/ait/202307100147.aspx?

M7. 2022: Synopsys Blog: Advancing STEM Education & Research with EDA Tools, 2022
https://www.synopsys.com/blogs/chip-design/stem-education-with-eda-tools.html

M8. 2022: Mercury News: The U.S. is bringing chip-making home. Is California ready? 2022
https://www.mercurynews.com/2022/09/04/the-u-s-is-bringing-chip-making-home-is-california-ready/
https://edition.pagesuite.com/tribune/article_popover.aspx?guid=8493b1f6-8be4-4874-9f51-cfeedf6a468a

M9. 2021: SJSU News Center: Electrical Engineering Faculty Receives NSF CAREER Award for Cryogenic Electronics Research
https://blogs.sjsu.edu/newsroom/2021/electrical-engineering-faculty-receives-nsf-career-award-for-cryogenic-electronics-research/

M10. 2021: Engineering Magazine: New Master's Specialization in Quantum Computing & Information
https://www.sjsu.edu/engineering/docs/magazines/SJSU_AlumniMagazine-Spring2021_Spreads_Web.pdf

M11. 2019: Engineering Magazine: Hiu-Yung Wong's Non-Traditional Path to Professorship (Fall 2019)
https://www.sjsu.edu/engineering/docs/magazines/fall-2019.pdf

Other Technical Publications

- Subrat Mishra, Narendra Parihar, Rakesh Rao, and Souvik Mahapatra, **Hiu Yung Wong**, Steve Motzny, and Victor Moroz, "NBTI Modeling in Sentaurus Device", Synopsys TCAD Newsletter December 2016.
- TCAD Application Note "Device Monte Carlo Simulation Methodology of Two-dimensional FinFET Slices", 2012
- TCAD Application Note "Simulation of Normally Off GaN MISFET with Piezo Neutralization Technique", 2011
- TCAD Application Note "Simulation of Normally Off AlGaN/GaN HFETwith p-Type GaN Gate and AlGaN Buffer", 2011
- SRC Report on tunable work function gate technology options (2-Aug-2004). Publication: P009712 (with K. Shin).
- 0.35um CMOS Process on Six-inch Wafers Baseline Report IV, A. Horvath, S. Parsa and **H. Y. Wong**, Memorandum No. UCB/ERL M05/15, Electronics Research Laboratory, College of Engineering, UC Berkeley
- **H Wong**, N Braga, S Tian, R Borges, "Simulations Enhance The Development Of Power Devices", compound semiconductor, 2011

Education

- **Program created:** Master of Science in Quantum Technology at San Jose State University, 2023
- **Specialization created:** Quantum Computing and Information Specialization, MS Electrical Engineering
- **Courses created**
  EE222, EE225, EE226, EE274
- **Lecturer**
  EE274. Quantum Computing Architectures, San Jose State University, (32 students), Spring 2025
  EE226. Cryogenic Nanoelectronics, San Jose State University, (19 students), Spring 2024
  Class and Lab Coordinator: EE124. Electronic Design II, San Jose State University, (74 students), Spring 2024
  EE225. Introduction to Quantum Computing, San Jose State University, (18 students), Fall 2023
  Class and Lab Coordinator: EE124. Electronic Design II, San Jose State University, (32 students), Fall 2023
  EE124. Electronic Design II, San Jose State University, (53 students), Spring 2023
  EE274. Quantum Computing Architectures, San Jose State University, (12 students), Spring 2023
  EE124. Electronic Design II, San Jose State University, (60 students), Fall 2022
  EE225. Introduction to Quantum Computing, San Jose State University, (24 students), Fall 2022
  EE124. Electronic Design II, San Jose State University, (52 students), Spring 2022
  EE226. Cryogenic Nanoelectronics, San Jose State University, (16 students), Spring 2022
  EE124. Electronic Design II, San Jose State University, (59 students), Fall 2021
  EE225. Introduction to Quantum Computing, San Jose State University, (14 students), Fall 2021
  EE124. Electronic Design II, San Jose State University, (57 students), Spring 2021
  EE224. High Speed CMOS Circuits, San Jose State University, (26 students), Spring 2021
  EE124. Electronic Design II, San Jose State University, (70 students), Fall 2020
  EE222. Advanced Integrated Device, San Jose State University, (16 students), Spring 2020
  EE124. Electronic Design II, San Jose State University, (57 students), Spring 2020
  EE225. Introduction to Quantum Computing, San Jose State University, (11 students), Spring 2020
  EE124. Electronic Design II, San Jose State University, (56 students), Fall 2019
  EE224. High Speed CMOS Circuits, San Jose State University, (18 students), Fall 2019
  EE124. Electronic Design II, San Jose State University, (58 students), Spring 2019
  EE222. Semiconductor Devices II, San Jose State University, (13 students), Spring 2019
  EE124. Electronic Design II, San Jose State University, (68 students), Fall 2018
  EE224. High Speed CMOS Circuits, San Jose State University, (31 students), Fall 2018

- **Teaching Assistant experience (from Devices to Digital/Analog Circuits to Computer Architectures):**
  Microelectronic Devices and Circuits (EE 105), EECS, UC Berkeley, Fall 2005
  Analog Integrated Circuits (EE 140), EECS, UC Berkeley, Fall 2001
  Computer System Architectures (CEG 3420), CSE, CUHK, Spring 2001
  Digital Circuits (CEG 3470), CSE, CUHK, Fall 2000
  Computer System Architectures (CEG 3420), CSE, CUHK, Spring 2000, ***Best TA Award***
  Digital Circuits (CEG 3470), CSE, CUHK, Fall 1999, ***Best TA Award***

- **10-year TCAD and device physics training experience to customers**