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A Simplified Algorithm For Efficient Power Characterization And Estimation

May Huang, Member IEEE, Raymond Kwok, Member IEEE, Shu-Park Chan, Fellow, IEEE

ABSTRACT

Accurate power analysis in the early design cycle can influence design decisions, especially in submicron designs. This paper introduces a novel and simplified algorithm, the Linear Power Equation (LPE), of the total average power calculation. The algorithm significantly simplifies the approach of power characterization for ASIC cells and examined by different types of ASIC cells with various manufacture technologies and processing conditions. The algorithm is implemented as a gate-level power analysis prototype to perform a simulation based, gate-level power estimation. Some experimental results are presented in the paper to assess the validity and feasibility of this approach.

1. INTRODUCTION

Power analysis in the early design cycle is becoming an important consideration in deep submicron designs. Engineers used to spend a long time to analyze the power consumption at the transistor-level in order to obtain reliable results. Due to the shortening of design cycles, designers can no longer wait for the transistor-level designs to be completed before performing power analysis. Searching for an accurate higher level power analysis method becomes a challenge for the design automation market. For gate-level power analysis, the core is how to process the internal power dissipation whose representation depends on the power characterization. Our focus here is to develop an efficient algo-

rithm of power estimation for ASIC designs, and associate power characterization approach.

There are two basic types of power dissipations at IC circuits: static and dynamic. The static power dissipation is very small in CMOS circuits because of the absence of DC paths. The dynamic power dissipation is composed of two terms: capacitive and short-current. The capacitive power dissipation is the summation of power dissipated at the external nets and the internal nodes of cells. We consider the internal capacitive and short-current power dissipations together as the internal power dissipation. The external capacitive power can be calculated by recording the switching activities and lumped capacitances at each individual net. Because the internal switching activities and short-current of a cell are invisible for ASIC customers or EDA tools, the current gate-level power analysis tools take into account the capacitive (switching) power dissipations at the nets, and leave rooms for ASIC vendors to represent internal power dissipations of the cells in the ASIC libraries. There are two common methods to represent the internal power dissipations. One is an I/O pin based representation which represents the internal power dissipation by either energy value or equivalent capacitance distributed to some input and output pins of a cell. The other is an event-based representation which represents the internal power in a table, in which each element corresponds to a set of input states. With these data, a gate-level power calculation tool can achieve an accurate power analysis. The accuracy depends on how accurate the internal power can be represented in the ASIC libraries.

Preparing data to represent the internal power of an ASIC cell is often referred to as power characterization which is usually based on SPICE simulation associated with the process of pattern preparation, simulation and parameter generation. There are various algorithms for power characterization such as ISM (Input Slope Modeling) of Compass and the DBT model [7]. We present a algorithm in this paper which reduce the power characterization effort significantly without scarifying the accuracy. The algorithm is applied to a gate-level power analysis and satisfied results are obtained from test circuits.

2. THE BACKGROUND

To provide proper parameters to represent the internal power accurately in an ASIC library, power analysis at transistor level based on circuit character is essential. We analyzed all different types of ASIC cells, based on their CMOS schematics and electrical characteristics, on different technologies and different processing conditions. Power values calculated from SPICE simulation are used as the standard for the accuracy analysis. Since power dissipation is test pattern dependent, it should be emphasized that the power discussed for the characterization in this paper is an average power based on an exhaustive functional test vector set. We examined the power dissipation of circuits on the output loads and input slopes, and compared the external capacitive power *Pce* with the total average power *Psp* calculated from SPICE simulation. Interesting enough both the ratio of *Pce* over *Psp*, or the relative error, $[(P_{ce} - P_{sp})/P_{sp}] \cdot 100\ \%$, present similar curves and seem to be universal regardless of the details of the cells. We illustrate the results of two cells along with different conditions and

technologies in the Figures 1 and 2 as examples. Fig. 1 gives the relative error of a D Flip-Flop with three different processing conditions. The curve with an extension "_01" indicated that the input slope is 0.1ns, and "_10" means 1.0ns. The "_ss", "_typ" and "_ff" denote the worst, typical and best processing conditions respectively. Fig. 2 illustrates the relative error of a full adder on 0.2ns input slope within 0.8um, 0.5um and 0.35um technologies.

Fig 1. Relative error of *Pce* vs. *Psp*

Fig. 2. Relative error of *Pce* vs. *Psp*

Both the error function, $[(P_{ce}-P_{sp})/P_{sp}]\cdot 100\ \%$, and the ratio, *Pce/Psp*, can be numerically fitted into a number of expressions such as the logarithmic function as shown in Figures 1 and 2. The origin of this logarithm dependence can be understood easily in terms of its power series expansion, which is similar to that of the ratio of two linear expressions. Linear approximations are plotted in Fig.3, same cell as in Fig. 1, for comparison.

Fig. 3. Linear approximations to the error function

The linearity of *Pce* is commonly recognized as $P_{ce} = \sum_L \frac{1}{2}\cdot C_L \cdot V^2 \cdot \frac{n}{T}$, where C_L is the capacitive loading at a net, n is the switching number, and T is the simulation period. It is also possible to approximate the total average power dissipated in the circuit to a linear function of the output loading. To study the validity of this approximation, we write the composition of a total power dissipation as:

$$P_{total} = \sum_i \left(\frac{1}{2} C_i V^2 f_i + P_{si}\right) + \sum_j \left(\frac{1}{2} C_j V^2 f_j\right) + \sum_o \left(\frac{1}{2} C_o V^2 f_o + P_{so}\right)$$

where: i is an internal node; j is an input net; and o is an output net; P_{si} and P_{so} represent short-current power dissipated at internal and external stages individually.

The power dissipation calculated in SPICE is:

$$P_{sp} = \sum_i \left(\frac{1}{2} C_i V^2 f_i + P_{si} + P_{so}\right) + \sum_o \left(\frac{1}{2} C_o V^2 f_o\right)$$

Since the input capacitive loadings consume power from the previous stage, the input capacitive power is not included in P_{sp}. The internal capacitive power, $P_{CI} = \sum_i \left(\frac{1}{2} C_i V^2 f_i\right)$, is not a function of output loading, therefore does not contribute to P_{sp}. Finally, the short-current power, $\sum (P_{si} + P_{so})$, is a function of the input slope, but almost independent on the output loading.

Based on the above analysis, the total power of a cell can be approximated by in a linear equation. This assumption has been proven by a host of examinations for ASIC cells. Figure 4 shows the relation of the power components of a cell. All these power values are measured in SPICE simulation. Curve P_{s01} and P_{s10} represent the short-current power corresponding to 0.1ns and 1.0ns input slope, and P_{h01} and P_{h10} represent the total power with respect to 0.1ns and 1.0ns input slope. The short-current power shown in Fig. 4 is almost a straight line along with the increase of the output load, so that the total power appears to be nearly linear.

Fig. 4. The relation of power components of an ASIC cell

Tests on different types of cells also come to a similar conclusion. The next two figures illustrate the behavior of the capacitive or total power dissipations of a cell as a function of its output loads. Fig. 5 shows the power property of a latch, and in Fig. 6, a 4-to-1 multiplexer.

Fig. 5. Power property of a latch

Fig. 6. Power property of a multiplexer

3. THE ALGORITHM

The algorithm developed is based on a linear approximation, named Linear Power Equation (LPE) to calculate the total average power dissipation of an ASIC cell in terms of the external capacitive power. As mentioned earlier, an external capacitive power is given by: $P_{ce} = \sum_{L} \frac{1}{2} \cdot C_L \cdot V^2 \cdot \frac{n}{T}$. For a single output cell, it can also be written as: $P_{ce} = ax + d$, based on its linear functionality with output load x. Actually the input capacitances of a cell, which contributed to d in the above expression, have been included in the previous stage capacitive power dissipation, therefore we consider the output capacitive loads only and the equation of P_{ce} is simplified to $P_{ce} = ax$. The total average power dissipation of a cell can be approximated as a linear function $P_T = gx + b$. The different between P_{ce} and P_T is the internal power dissipation. The parameters a, b and g can be extracted by simulations. The rest of the paragraph gives the equations to calculate a single- and a multi-output ASIC cell as well as practical approach to derive parameters a, b and g.

One way to define the LPE for a single output cell is:

$$P_{ce} = ax = P_{CE1.0}$$

$$P_T = gx + b = (P_{SP1.0} - P_{SP0.2})/(1.0 - 0.2) \cdot x + (P_{SP1.0} - P_{CE1.0})$$

where P_T is the total power; $P_{CE1.0}$ is the external capacitive power with output loading 1.0pf; $P_{SP1.0}$ is the average power calculated in SPICE simulation with 1.0pf on output loading; $P_{I1.0}$ is the internal power at the same condition.

The corresponding LPE for a m-output cell is:

$$P_T = G^{\tau}X + JB = \sum_{i=1}^{m} ((P_{SPi1.0} - P_{SPi0.2})/(1.0 - 0.2))x_i + \frac{1}{m}\sum_{i=1}^{m} (P_{SPi1.0} - P_{CEi1.0})$$

where G, X and B are vectors with m elements, and J is a 1 by m matrix with all elements equal to "1". $P_{CEi1.0}$ represents the capacitive power when output i is assigned to 1.0pf and other outputs are 0 load. Correspondingly, $P_{SPi1.0}$ and $P_{SPi0.2}$ are the power calculated in SPICE with 1.0pf and 0.2pf loading at output i, and 0 loading at other outputs. The character τ is denoted as the transpose of the matrix.

To simplify the process further, one can use an unified slope of LPE, i.e. to equate the slope of P_{ce} and P_T since they are typically very close according to our experiments. Therefore, the equation of P_T can be written as $P_T = ax + b$. Refer to Figs. 3 and 4, *F1(x)* in Fig. 3 is defined as $F1(x) = ((P_{ce} - P_T)/P_T) \cdot 100\%$, where $P_{ce} = ax + d$ and $P_T = gx + b$, so that

$$F1(x) = \{[(ax + d) - (gx + b)]/(gx + b)\} \cdot 100\ \% = \{[(a - c)x + (d - b)]/(gx + b)\} \cdot 100\ \%.$$

F2(x) in Fig.4 is derived based on the unified slope of LPE where $a = g$.

4. THE CHARACTERIZATION

Characterization of ASIC cells is a complex work regardless the details of timing or power. But it is very important, since the accuracy of a circuit analysis depends on it. We introduce an approach of power characterization based on the above algorithm. Since the power of each cell is the function of input slope, output loads, and a test vector set, providing the complete combination for these three variables, a table of power parameters will be a large one even for a small cell. The size of the table will effect the efficiency of the power analysis. To provide a rational parameter table is the challenge of power characterization. This paper does not focus on the optimization of a power table but instead, introduces an novel approach which significantly reduces the efforts of power characterization and support an efficient power analysis. The variables needed for LPE power characterization are *A*, *B* and *G* depending on the complexity of a cell. The following formulas summarize their definitions:

$$a_i = P_{CEi1.0}\Big|_{condi}, \qquad a_i \in A, \qquad i \in \{1, \cdots, m\};$$

$$b_i = \frac{1}{m}(P_{SPi1.0} - P_{CEi1.0})\Big|_{condi}, \qquad b_i \in B, \qquad i \in \{1, \cdots, m\}$$

$$g_i = (P_{SPi1.0} - P_{SPi0.2})\Big|_{condi}, \qquad g_i \in G, \qquad i \in \{1, \cdots, m\}$$

$$P_{CEi1.0}\Big|_{condi} = \frac{1}{2} \cdot c_i \cdot V^2 \cdot \frac{n_i}{T}\Big|_{c_i = 1.0pf,\ c_j = 0,\ j \neq i,\ i,j \in \{1, \cdots, m\}}$$

$$P_{SPi1.0}\Big|_{condi} = (I_{avg} \cdot V)\Big|_{c_i = 1.0pf,\ c_j = 0,\ j \neq i,\ i,j \in \{1, \cdots, m\}}$$

$$P_{SPi0.2}\Big|_{condi} = (I_{avg} \cdot V)\Big|_{c_i = 0.2pf,\ c_j = 0,\ j \neq i,\ i,j \in \{1, \cdots, m\}}$$

Parameters a, b and g can be considered as a special subset of A, B and G. An exhaustive functional test vector set is used during the simulation. Two SPICE simulations are required for a defined input slope to obtain $P_{SP1.0}$ and $P_{SP0.2}$. The switching activities of the output can be easily recorded, so that the parameter $P_{CE1.0}$ is acquired. A combinational cell with m outputs requires $2m$ times of SPICE simulation, each produces a couple $P_{SPi1.0}$ and $P_{SPi0.2}$ (i from 1 to m). Power values obtained from simulations can be parameterized as either energy values or equivalent capacitances. One or more tables can be constructed for a cell after the characterization. If using an unified slope of LPE, the characterization can be reduced to one SPICE simulation for a single-output cell, and m times for a m-output cell.

For a sequential cell, more considerations are applied. For example, a D Flip-Flop requires more parameters to represent some special situations, such as the clock rests but the data toggling or vise versa. In these cases, the output of DFF does not change so that the parameter derived from the above equations cannot cover the situation here. Extra parameter table is required for a sequential cell.

5. THE POWER ESTIMATION

There are two types of analysis for power estimation of a given circuit: simulation based and probability based. There are many references on the statistical power estimation approach ([5],[7],[8],[11]). We concentrate on a simulation based power analysis in this paper.

To process internal power, P_I, is the core in gate-level power analysis. Normally ASIC vendors perform the cell characterizations to determine either the internal power and represent them in LUTs (Look-Up Tables), or the internal power parameters and use them in formulas.

Mapping the internal power to energy tables can be implement in different ways. There are two major methods for representing the internal power in energy tables.

1. The first one identifies an energy value to an associate primitive pin of a cell. Whenever the pin is switched, the attached internal energy is counted. This method reflects the internal power into the input/output pins. In another words, it converts the internal power into an equivalent external capacitive power. One cell may have more than one energy table being attached. With this method, only the switching activities at each net would be recorded.

2. The second one is an event-based power description which defines an energy associated with a set of input states. There may be a huge table if considering all possible input-state combinations, so some trade-off is necessary. With this method, not only the switching activity at each net should be watched, but also the input states of each cell should be examined to determine which energy element should be chosen. Therefore this method may slow down the simulation process comparing to the previous one.

The following equation shows how an energy value is derived and used for power calculation,

$$P_2 = \left(P_1 \cdot \frac{T_1}{n_1}\right) \cdot \frac{n_2}{T_2} = E \cdot \frac{n_2}{T_2}$$

where subscripts 1 and 2 indicate two different simulation environments.

To implement the LPE to gate-level power analysis, the power characterizations for ASIC cells are performed as described in the above section. The obtained parameters can be placed into a LUT, either using *A*, *B*, *G* directly, or adjusting them to an energy form such as *(ai * k)*, *(bi * k)*, and *(gi * k)*. For a single-output cell, the power dissipation can be calculated as:

$$P = [(gx + b) \cdot k] \cdot f = (gx \cdot k) \cdot f + (b \cdot k) \cdot f = \frac{1}{2} x V^2 \cdot f + E \cdot f, \qquad k = \frac{T_0}{n_0}, \qquad f = \frac{n}{T}$$

where *To* is the simulation period and *no* is the output switching number when deriving *g* and *b*. This equation shows that a power consists of two parts: capacitive and internal. The capacitive power can be calculated by $P_{ce} = ax \cdot k \cdot f$ or $P_{ce} = \frac{1}{2} x \cdot V^2 \cdot f$.

The general equation for power calculation of an ASIC cell is:

$$P = (G_{mm} X)^{\tau} \cdot (K_{mm} F) + B^{\tau} (K_{mm} F)$$

$$= \left(\begin{bmatrix} g_1 & & & \\ & g_2 & & \\ & & \ddots & \\ & & & g_m \end{bmatrix} \cdot \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_m \end{bmatrix} \right)^{\tau} \cdot \left(\begin{bmatrix} k_1 & & & \\ & k_2 & & \\ & & \ddots & \\ & & & k_m \end{bmatrix} \cdot \begin{bmatrix} f_1 \\ f_2 \\ \vdots \\ f_m \end{bmatrix} \right) + \begin{bmatrix} b_1 & b_2 & \cdots & b_m \end{bmatrix} \cdot \left(\begin{bmatrix} k_1 & & & \\ & k_2 & & \\ & & \ddots & \\ & & & k_m \end{bmatrix} \cdot \begin{bmatrix} f_1 \\ f_2 \\ \vdots \\ f_m \end{bmatrix} \right)$$

$$= \sum_{i=1}^{m} g_i \cdot x_i \cdot k_i \cdot f_i + \frac{1}{m} \sum_{i=1}^{m} b_i \cdot k_i \cdot f_i$$

$$= \sum_{i=1}^{m} g_i \cdot x_i \cdot k_i \cdot f_i + \sum_{i=1}^{m} E_i \cdot \frac{n_i}{T},$$

Using the unified slope of LPE, the above equation is simplified as:

$$P = (A_{mm}X)^{\tau} \cdot (K_{mm}F) + B^{\tau}(K_{mm}F)$$

$$= \sum_{i=1}^{m} \frac{1}{2} x_i V^2 \cdot \frac{n_i}{T} + \sum_{i=1}^{m} E_i \cdot \frac{n_i}{T},$$

During a simulation, the switching activity and lumped capacitive load at each net can be recorded into a file through PLI. For power analysis using a functional test vector set, the above equation is applied. In some special cases, such as a partial circuit rests in order to saving power within a low power design, the associate extra table of a sequential cell has to used to implement the special power consumption.

A dialog of a simulation based gate-level power analysis is shown in Figure 7. The flow demonstrates the considerations and interfaces of a power analysis tool in a design flow.

Figure 7. Gate-level Power Analysis

The external capacitive powers are calculated, and the internal powers are estimated using the power library. Therefore, the dynamic power dissipations in a given design can be analyzed.

6. TEST CASES

We implemented the LPE into a tool prototype, and used it on power characterization to construct a power library, then perform the gate-level power analysis. Two test circuits are shown below as examples to demonstrate the power analysis using the unified slope of LPE. The results are compared with the val-

ues from SPICE to show the accuracy.

The first test circuit is a12-bit counter which contains 30 different types of ASIC cells, about 120 number of cells or over 1250 transistors. A functional test vector set is used in the simulation. The result of the power analysis is listed Table 1.

Power in Hspice Psp	Power in Prototype Ppt	Error % (Ppt-Psp) / Psp
1264.989 uw	1239.919 uw	-1.98 %

Table 1: Power Analysis Results of Test Circuit 1

The second test circuit is an alarm-clock circuit with scan-chains which contains 65 different types of cells, about 500 number of cells or over 4200 transistors. The result of the power analysis is listed Table 2.

Power in Hspice Psp	Power in Prototype Ppt	Error % (Ppt-Psp) / Psp
2097.777 uw	2020.988 uw	-3.66 %

Table 2: Power Analysis Results of Test Circuit 2

The power analysis results of the two test circuits are very close to the SPICE results because the internal powers are modeled accurately within a library. Successfully representing the internal power dissipations establish the accuracy of the gate-level power analysis.

7. CONCLUSIONS

A new algorithm LPE is proposed for the total average power calculation. This algorithm is implemented by a linear approximation so that the process of power characterization is simplified significantly. The methodology is accom-

plished by a prototype which is used for power characterization, library development and gate-level power estimation. The LPE is examined by test circuits and obtained high accuracy comparing to the HSPICE result. Using the unified slope of the LPE further simplify the power characterization approach. However to improve the accuracy of the LPE, one should abandon the simple substitution of the linear coefficients a and g, and derive them precisely and separately.

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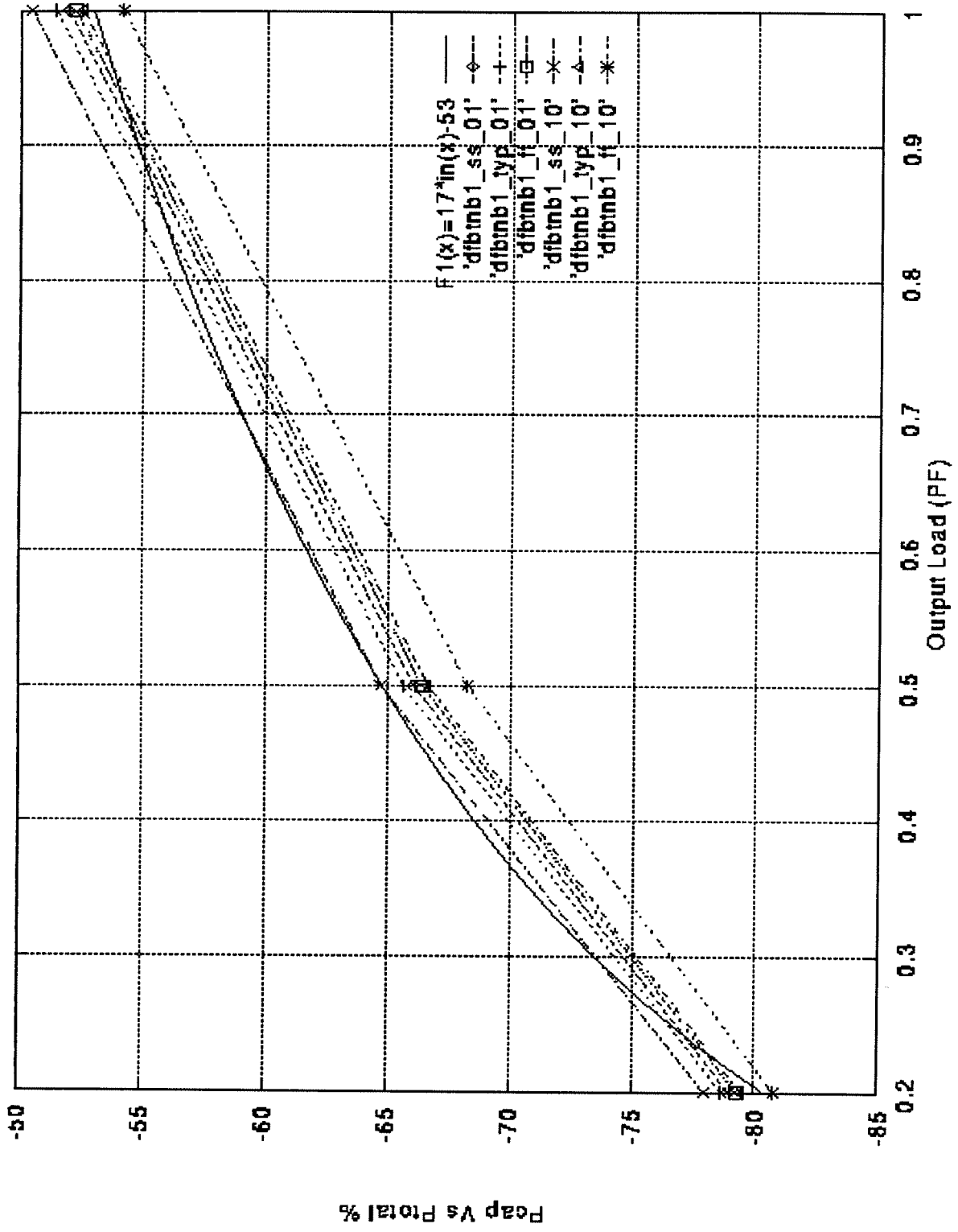

Fig 1. Relative error of P_{ce} vs. P_{sp}

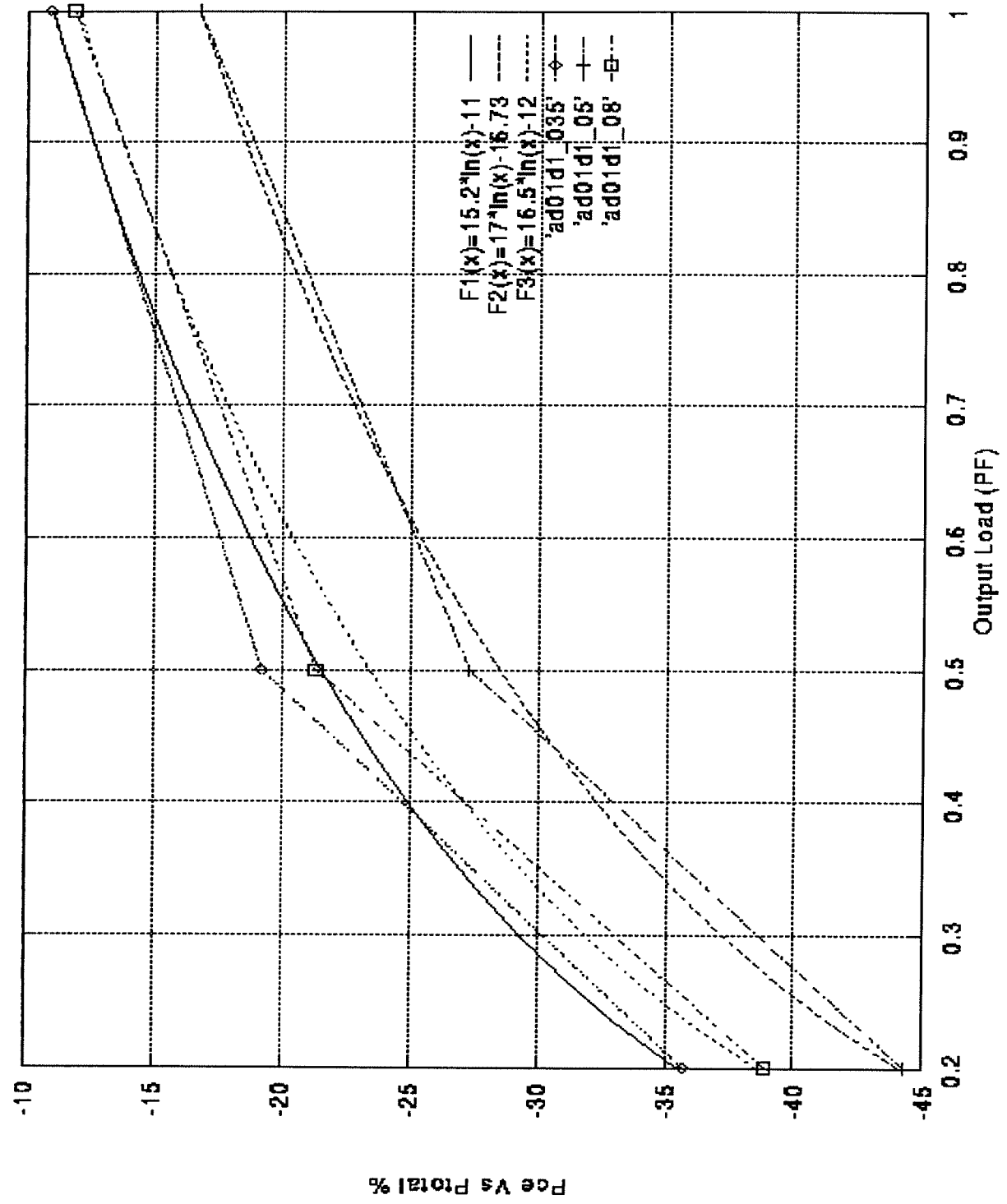

Fig. 2. Relative error of *Pce* vs. *Psp*

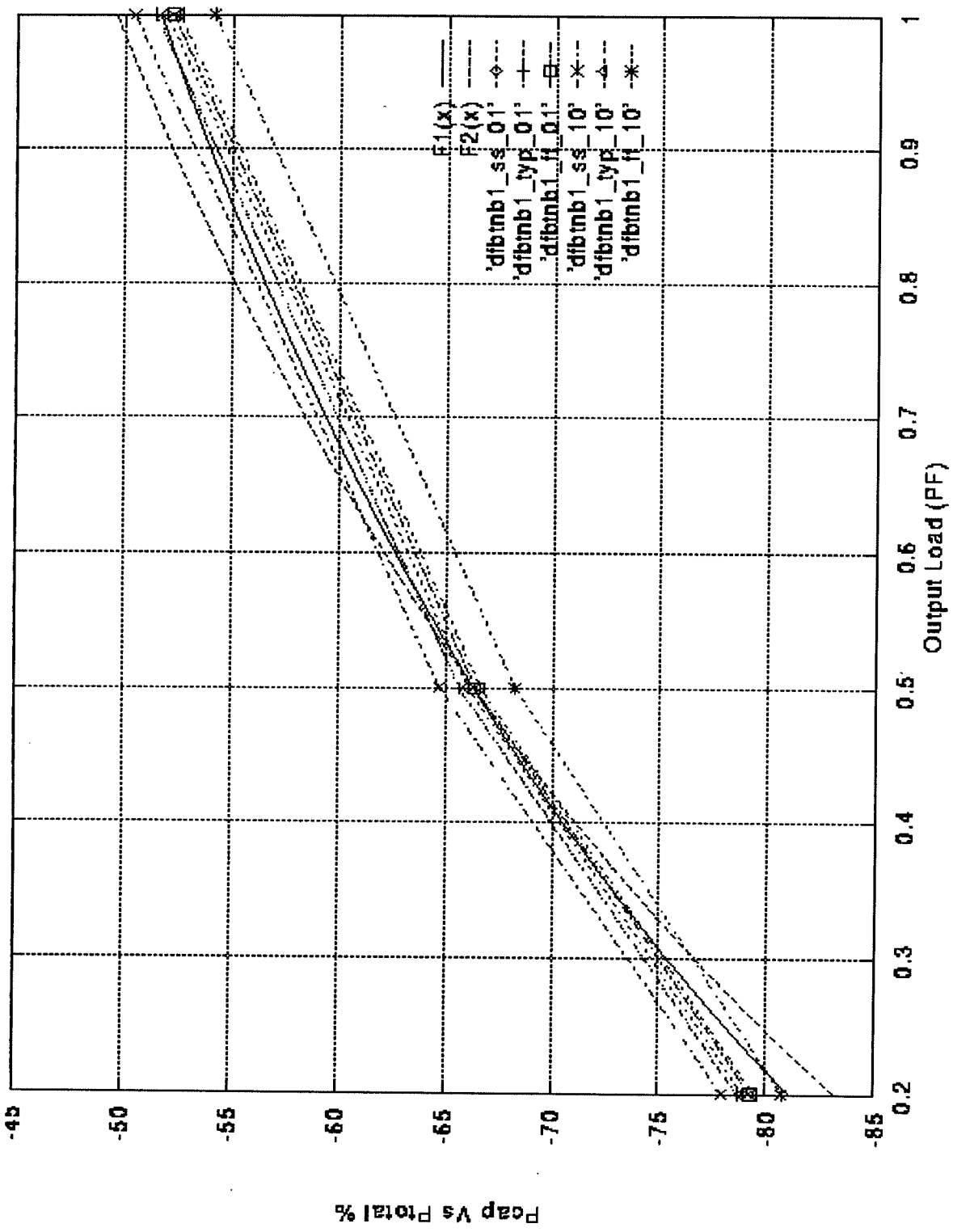

Fig. 3. Linear approximations to the error function

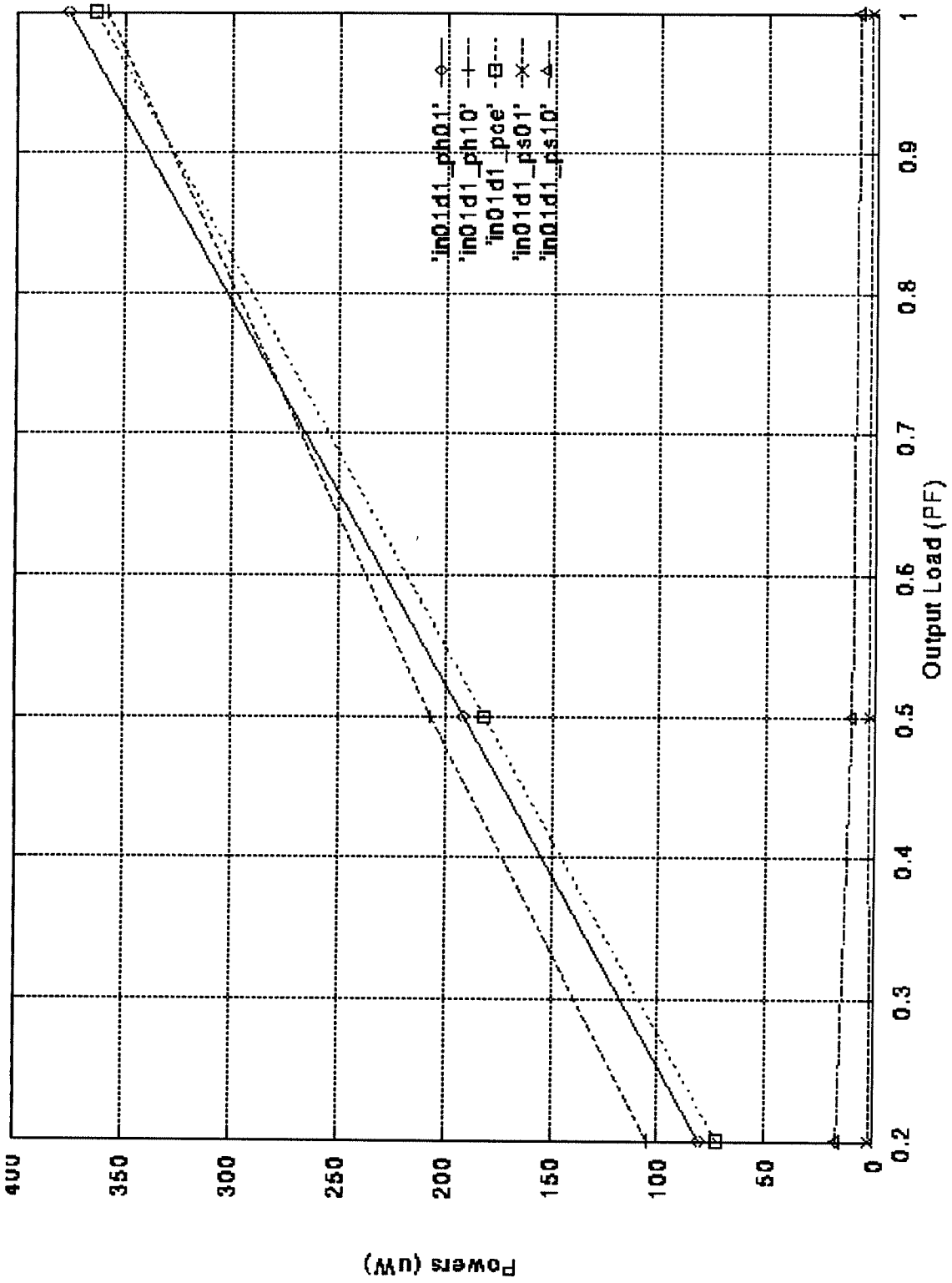

Fig. 4. The relation of power components of an ASIC cell

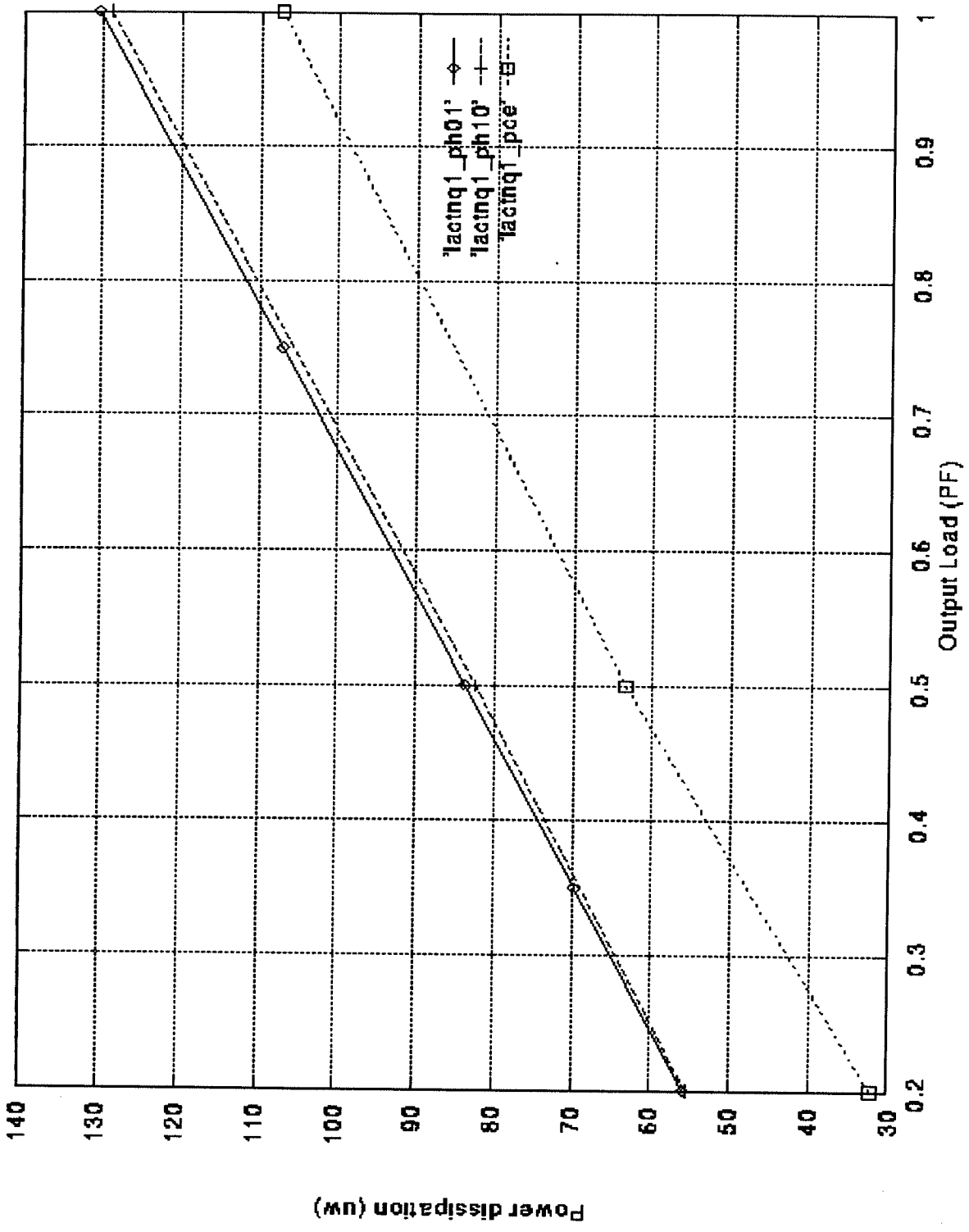

Fig. 5. Power property of a latch

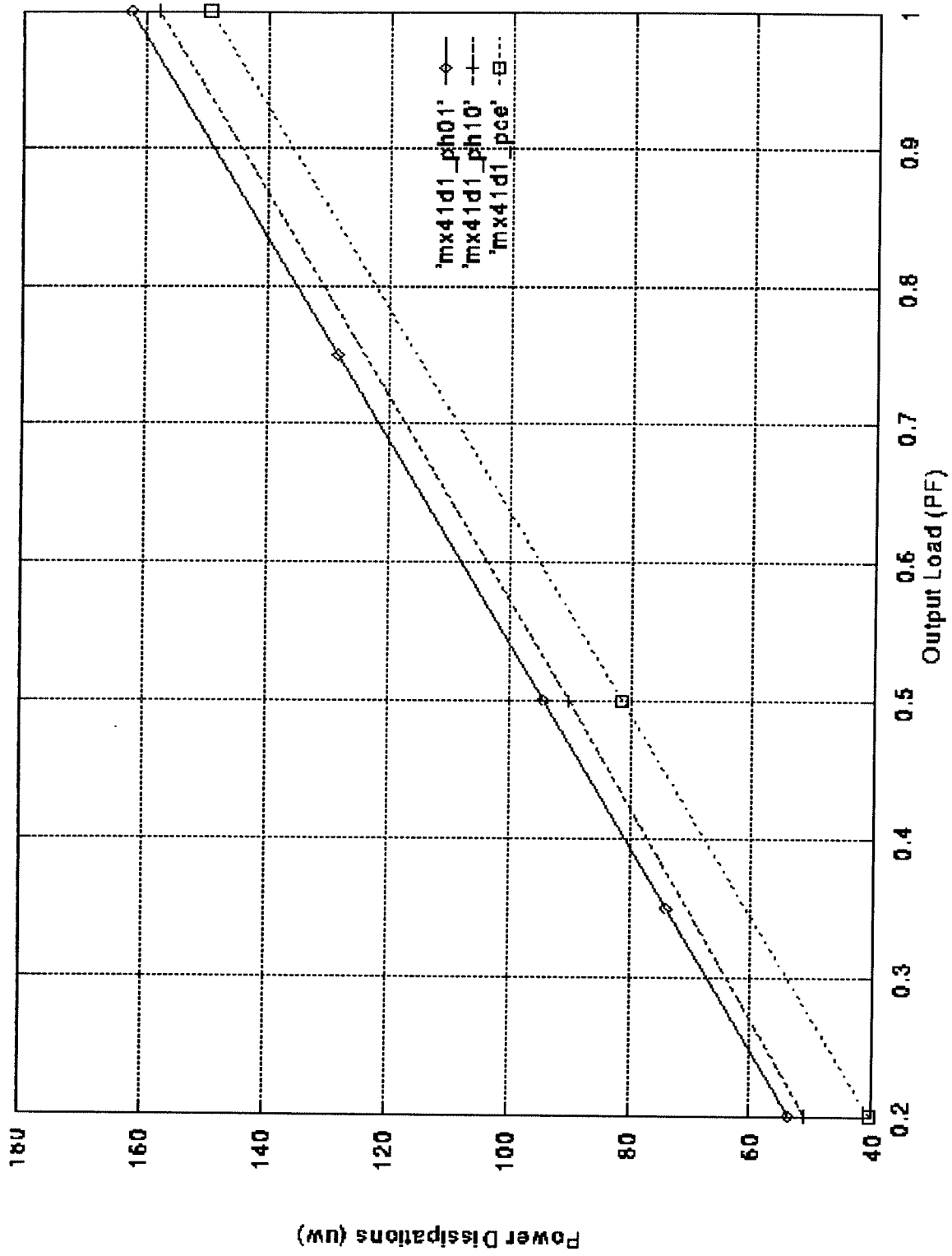

Fig. 6. Power property of a multiplexer

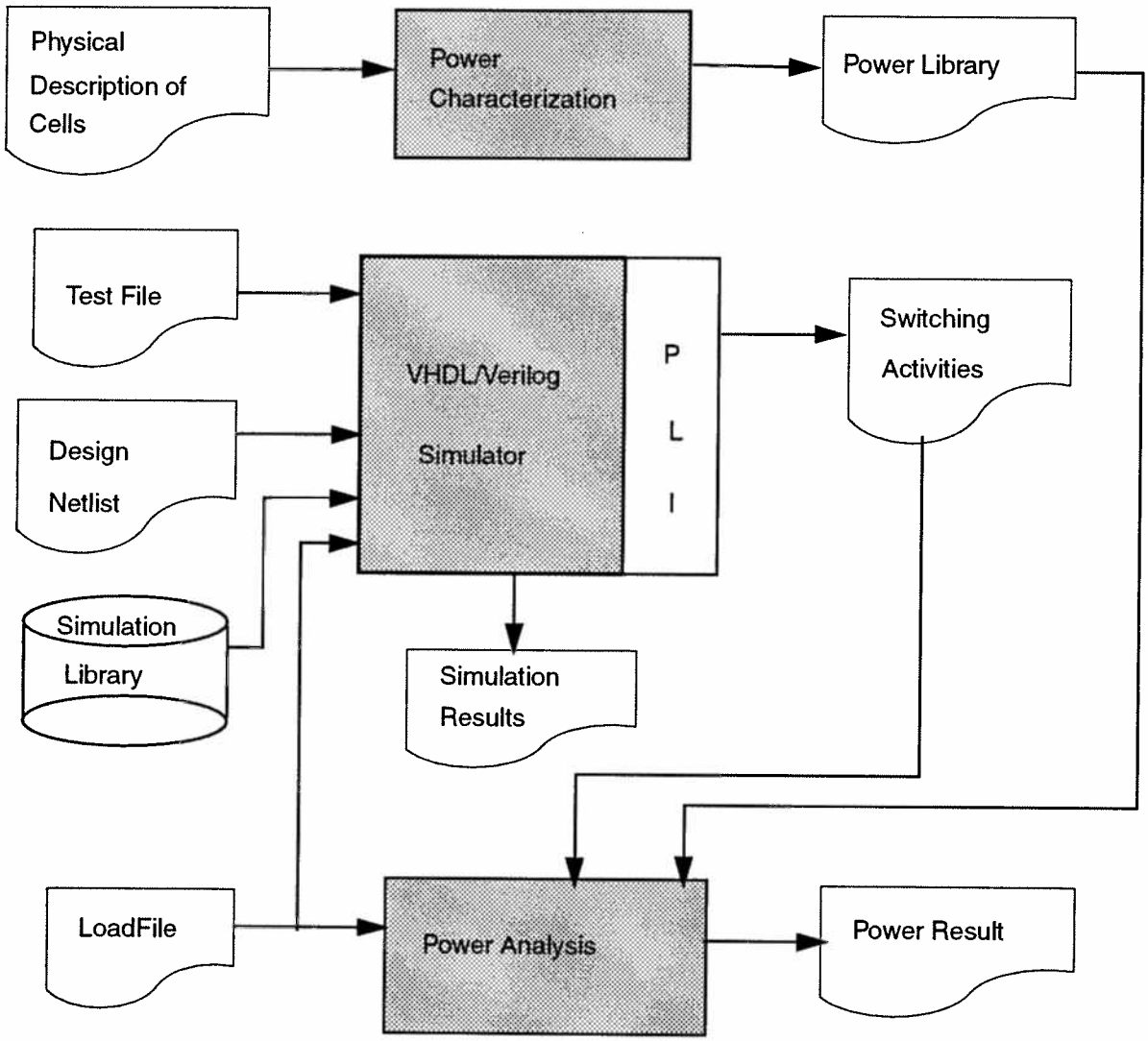

Figure 7. Gate-level Power Analysis